PIEZOELECTRIC THIN FILMS AND NANOWIRES: SYNTHESIS AND CHARACTERIZATION

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PIEZOELECTRIC THIN FILMS AND NANOWIRES: SYNTHESIS AND CHARACTERIZATION

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To my entire family and friends

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SUMMARY

Piezoelectric materials are widely used for sensors, actuators and trasducers. Traditionally, piezoelectric applications are dominated by multicomponent oxide ferroelectrics such as lead zirconate titanate (PZT), which have the advantage of high piezoelectric coefficients. Recently, one-dimensional piezoelectric nanostructures such as nanowires of zinc oxide (ZnO) and gallium nitride (GaN) has gained a lot of attention due to their combined piezoelectric and semiconducting properties. The focus of this thesis is to study the processing and electric properties of such piezoelectric thin films and nanostructures for various applications.

There is an increasing interest to form thin films of multicomponent ferroelectric oxides such as PZT on three-dimensional structures for charge storage and MEMS applications. Traditional vapor phase deposition techniques of PZT offer poor conformality over three-dimensional surfaces due to their reactant transport mechanisms. As an alternative, sol-gel synthesis may provide new process possibilities to overcome this hurdle but the film quality is usually inferior, and the yield data was usually reported for small device areas. The first part of this study is dedicated to the characterization of the electric properties and yield of PZT thin film derived from the sol-gel process. PZT thin films with good electric property and high yield over a large area have been fabricated. La doping was found to double the breakdown field due to donor doping effect. $LaNiO_3$ thin films that can be coated on a three-dimensional surface have been synthesized by an all-nitrate based sol-gel route, and the feasibility to form a conformal coating over a three-dimensional surface by solution coating techniques has been demonstrated.

ZnO and GaN micro/nanowires are promising piezoelectric materials for energy harvesting and piezotronic device applications. The second part of this study is focused

on the growth of ZnO and GaN micro/nanowires by physical vapor deposition techniques. The morphology and chemical compositions are revealed by electron microscopy. Utilizing the as-grown ZnO nanowires, single nanowire based photocell has been fabricated, and its performance was studied in terms of its response time, repeatability, excitation position and polarization dependence upon He-Cd UV-laser illumination. The excitation position dependence was attributed to the competition of two opposite photo- and thermoelectric currents originated from the two junctions. The excitation polarization dependence was attributed to the difference in optical properties due to crystallographic anisotropy. Employing the as-grown GaN nanowires, single nanowire based strain sensor is demonstrated, and its behavior is discussed in terms of the effect of strain-induced piezopotential on the Schottky barrier height.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Piezoelectric materials are widely used for sensors, actuators, and transducers [1]. Traditionally, piezoelectric applications are dominated by ferroelectric oxides such as lead zirconate titanate (PZT), which have the advantage of high piezoelectric coefficients. Recently, research on piezoelectric nanowires such as zinc oxide (ZnO) and gallium nitride (GaN) has gained a lot of attention due to their combination of piezoelectric and semiconducting properties [2, 3]. It is therefore desirable to study the process of both material forms and also compare their pros and cons for device applications.

The objective of this study is to systematically study the materials synthesis, device fabrication as well as characterization of the two types of systems.

1.2 Motivation and Objectives

1.2.1 Motivations and Objectives for PZT Thin Film Fabrication

1.2.1.1 3-D Ferroelectric Thin Film Capacitors for Decoupling and Energy Storage Applications

Figure 1.1 shows the summarized experimental data of breakdown field and dielectric constants for a variety of materials [4]. The maximum energy density stored in a dielectric material is a constant value, as given by the empirical relationship

$$\varepsilon_r E_{BR}^2 = 400$$

where ε_r is the dielectric constant and E_{BR} is the breakdown field. Therefore, there is a tradeoff between the desirable electrical properties and good reliability.

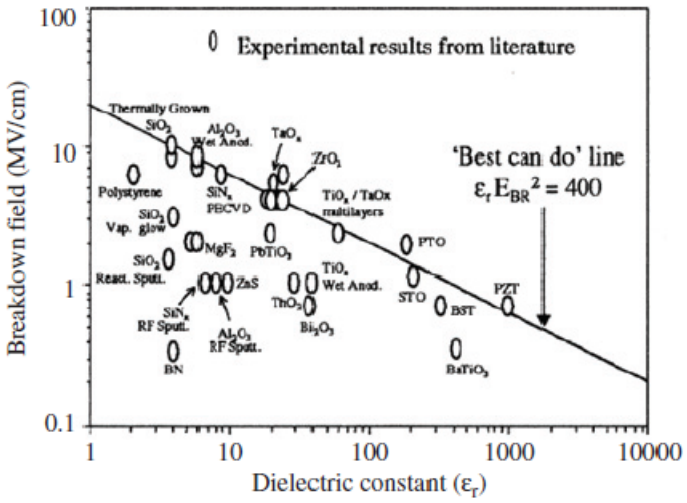


Figure 1.1 Breakdown field as a function of dielectric constants for a variety of thin films [4]

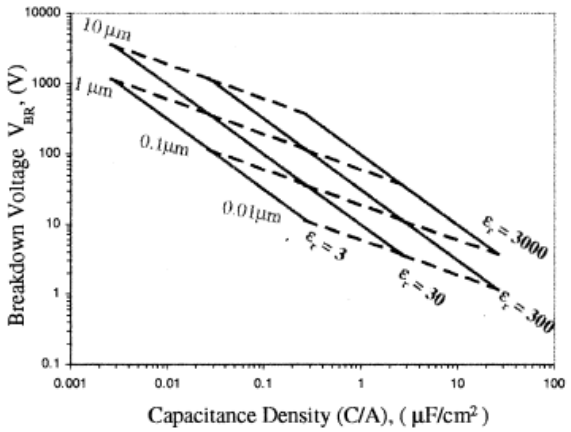


Figure 1.2. Breakdown voltages as a function of capacitance density in terms of dielectric constant and thickness [4]

Out of all available dielectric materials, oxides and nitrides with low dielectric constants have the highest breakdown fields. These materials usually have dielectric constants in the range of 4-7. According to the empirical relationship between breakdown voltages and capacitance densities, shown in figure 1.2 [4], the capacitance density for thin films with such materials is limited to 0.1-0.2 μF/cm^2.

High capacitance density ferroelectrics with permittivity of 500-1000 are therefore preferred for energy storage applications. However, there are several constraints that limit the feasible capacitance density to 2-3 $\mu F/cm^2$ [5]:

(1) Lower breakdown fields of 200-500 kV/cm compared to low dielectric constant materials, which requires thicker films for satisfying reliability [4]
(2) Susceptibility to defects that leads to leaky and lossy films [6]
(3) Interfacial defects or reactions that lead to a lower effective dielectric constant

Therefore existing thin film capacitors with a planar geometry, even with high dielectric constant ferroelectrics, does not present sufficient capacitance density as the device size shrinks.

A viable solution is to integrate the device structure onto 3-D platforms such as trenches which increases the effective device area without consuming extra system real estate. Trench capacitors were first introduced in the 1980s for DRAM capacitors. Such devices, however, employ low dielectric constant materials, and their fabrication is mostly dependent on costly vapor phase deposition tools such as ALD. A low-cost, high throughput approach to fabricate such 3-D structures is therefore highly desirable.

1.2.1.2 3-D Ferroelectric Thin Film Processing Techniques for Piezoelectric Applications

Energy harvesting and actuating applications of silicon cantilever based ferroelectric thin films are mostly based on the bimorph structure [7], in which a layer of ferroelectric thin film is sandwiched between two conducting electrode layers. This utilizes the d_{31} mode of the piezoelectric material, in which the material deformation direction is perpendicular to the charge generation direction.

A more efficient design for energy conversion applications is to use the d_{33} mode in which the charge generation is in the same direction as the material deformation. For ferroelectric materials, the value of d_{33} is 2-3 times higher than d_{31}. An example of such a design is shown in figure 1.3 [8]. However, in such a design the electric field distribution is non-uniform, which does not exploit the potential maximum energy conversion of the material.

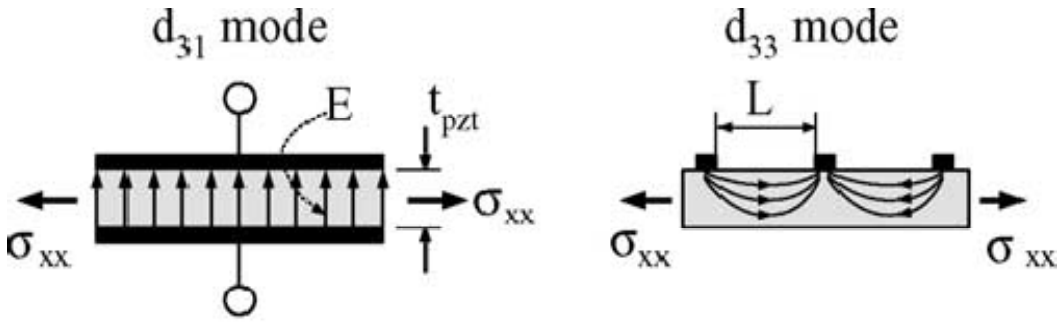


Figure 1.3 Example of designs for two piezoelectric modes for energy generation [8]

An alternative can be 3-D coatings on Si trench structures fabricated on a cantilever, with a filling material that fills the trench on top of the top electrode layer. In this structure, the portion of thin film coated on the vertical sidewalls of the trench can work under d_{33} mode while the horizontal portion works under d_{31} mode. An example of such a structure is shown in figure 1.4. Therefore, a feasible technique to integrate piezoelectric films on a silicon based 3-D platform is highly desirable.

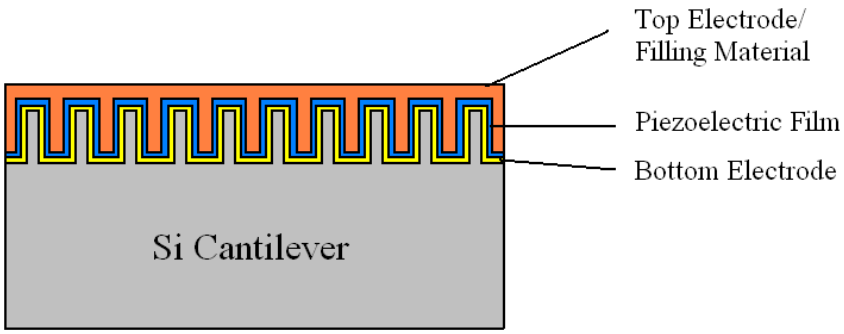


Figure 1.4 Proposed design of 3-D trench structure on a silicon cantilever for piezoelectric applications utilizing d_{33} mode

1.2.1.3 Proposed Chemical Solution Deposition for Fabrication of 3-D Ferroelectric Thin Film and Electrode Stacks

Chemical solution deposition techniques offer a low-cost approach to deposit complex oxide thin films. Traditionally, solution deposition is limited to planar surfaces and thin film formation is done using spin-coating. To address this limitation, this study proposes an alternative technique to fabricate devices on a 3-D surface with common spin-coating tools.

1.2.1.4 Objectives of Fabrication of 3-D Ferroelectric Thin Film and Electrode Stacks

The objectives of this study are to develop novel processes to enable integration of PZT and PLZT ferroelectric thin films onto 3-D surfaces, with the benefit of higher surface area for capacitor/memory applications and high versatility for MEMS applications. The objectives and targets for this research are:

Si and PZT compatible 3-D Electrode

(1) Explore the suitable material that is compatible with the Si technology and PZT material processing, while it can be conformally coated onto a 3-D surface.

(2) Explore, develop and evaluate a fabrication process and demonstration of the 3-D surface coating technique.

(3) Characterization of the conductivity of the electrode material.

Sol-gel Process of PZT/PLZT Thin Films

(1) Achieve high quality PZT/PLZT thin films suitable for capacitor/MEMS applications, which are characterized by a high capacitance density of 2-3$\mu F/cm^2$ at 100 kHz, and a breakdown voltage of greater than 10 V on 3 mm^2 planar devices, with a reasonable yield.

(2) Demonstrate process compatibility with 3-D surface coating, two methods of 3-D electrode fabrication are considered in this study to achieve the above mentioned objectives: (a) Process compatibility test of PZT with Nickel, which can be deposited onto a 3-D surface by electroplating, and (b) Process development of sol-gel conducting oxide electrode $LaNiO_3$, and evaluation of the possibilities to coat the liquid phase sol onto a 3-D surface conformally.

1.2.2 Motivations and Objectives for ZnO and GaN Nanowire Device Fabrication

1.2.2.1. Motivations for ZnO Microwire Photocell Measurement

Single ZnO microwire based photocell has been reported to produce opposite current when the microwire was illuminated at the two junctions, as shown in figure 1.5 [9]. This phenomenon was attributed to the opposite direction of local electric field of the two Schottky barriers formed at the junctions. The reference however only reported three illustration positions: at the two junctions, and on the body of the microwire near the center. It is therefore interesting to explore the photoresponse of the ZnO microwire device illustrated at other positions of the wire to evaluate the possible contribution of the local electric field.

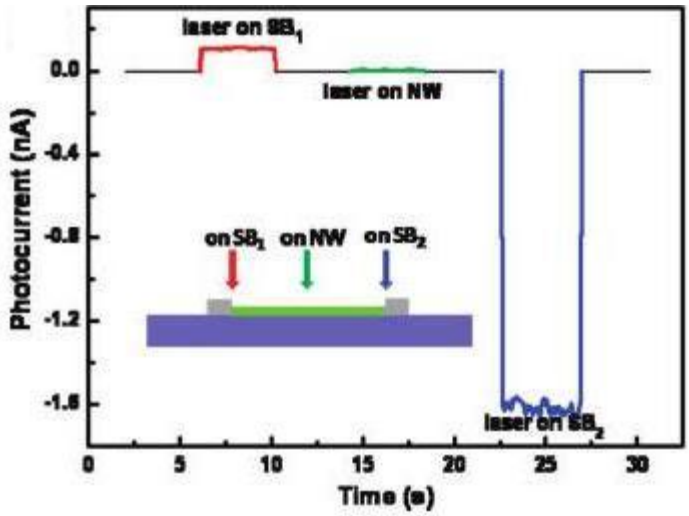


Figure 1.5 Measured photocurrent of a single ZnO microwire at the two junctions [9]

Optical effects in nanowires have been reported to be polarization dependent. Polarized light detection has been reported for thin ZnO nanowires with the diameter less than the excitation wavelength [10]. This effect was attributed to attenuation of the electric field in the thin wire direction which leads to a reduction of photocurrent when the polarization direction is perpendicular to the nanowire axis. It is still unclear if the photoresponse of a thick wire whose diameter exceeds the excitation wavelength still exhibit this polarization dependence. Therefore it is interesting to explore the situation in which a thick microwire of ZnO is excited with different polarized light.

1.2.2.2. Motivations for GaN Nanowire Synthesis and Strain-sensitive Single Nanowire Device Measurement

It has been reported that the I-V characteristics of a single ZnO nanowire connected by two electrodes with at least one Schottky contact can be tuned by the strain applied to the nanowire [11]. The mechanism was attributed to the change in Schottky barrier heights due to the strain-induced piezopotential.

Theoretical calculations on GaN nanowires have shown that the similar effect can exist for GaN nanowires as well, due to its similar crystal structure as ZnO which leads to piezoelectricity [12]. However, the effect of strain on a single GaN nanowire device has not been reported before. It is therefore highly desirable to synthesize GaN nanowires and test their response to strain when connected by two electrodes.

1.2.2.3 Objectives for ZnO and GaN Nanowire Device Fabrication and Measurement

Fabrication and Measurement of ZnO Microwire Photocell

(1) Explore the excitation position dependence of the ZnO microwire photocell and discuss the possible mechanisms that lead to this dependence

(2) Measure the photocurrent with different excitation polarizations and discuss the possible mechanisms that lead to this dependence

Fabrication and Measurement of Strain Sensitive GaN Nanowire Device

(1) Synthesize GaN nanowires with sufficient length that can be contacted with two electrodes.

(2) Measure the I-V characteristics of the GaN nanowire devices as a function of applied strain.

CHAPTER 2

SYNTHESIS OF FERROELECTRIC PZT AND PLZT THIN FILMS ON VARIOUS SUBSTRATES

2.1 Background

2.1.1 Crystal Structure and Properties

2.1.1.1 Crystal Structure of PZT

Lead zirconate titanate (PZT) and Lead lanthanum zirconate titanate (PLZT) ceramics have perovskite structure as shown in figure 2.1 [13]. The Pb^{2+} occupies the 8 corners and O^{2-} occupies the 6 face centers, while Zr^{4+} and Ti^{4+} sit inside the oxygen octahedral. When the position of the center ion shifts from the geometric center of the lattice, the centers of positive and negative ions no longer overlap, and spontaneous polarization arises.

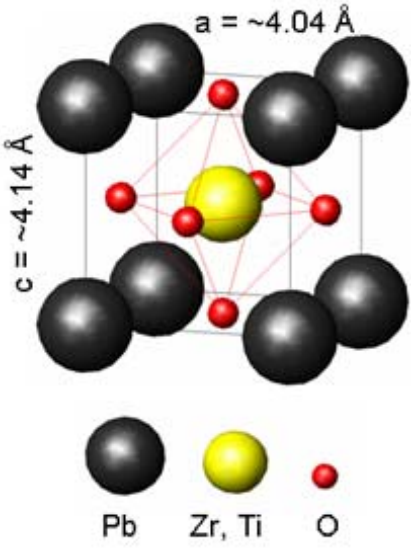


Figure 2.1 Crystal Structure of PZT [13]

PZT is one of the most widely used ferroelectric and piezoelectric materials. Ferroelectrics are defined as materials with switchable spontaneous polarization [1],

which means that the spontaneous polarization caused by relative displacement of the center of positive and negative charges can be reversed by an external electric field.

The relative displacement of the center of positive and negative charges is a result of both local field and elastic energy. The driving force for the displacement of an ion is the local field produced by the sum of the effects by all the dipoles around the ion. As the ion shifts, elastic energy increases and the balance of the two factors gives the equilibrium position of the ion.

2.1.1.2 Curie Temperature

At elevated temperatures, the lattice vibration will break up the center ion shift and thus the ferroelectricity, and the material becomes paraelectric. The temperature at which ferroelectricity breaks down is defined as the Curie temperature T_c. The reciprocal of the permittivity is linear with the temperature over a wide range in the paraelectric phase (Curie-Weiss law),

$$\varepsilon = \frac{C}{T - T_0}$$

C being the Curie-Weiss constant and T_0 being the Curie-Weiss temperature. For most ferroelectrics the value T_0 is slightly lower than the actual phase transition temperature T_c [1].

2.1.1.3 Domain Formation and Reorientation

Due to the combined influence of elastic and electric energies, ferroelectric grains are always split into many domains within which the polarization direction is the same. The polarization directions of all the domains are, under normal conditions, randomly distributed which result in zero net polarization. The material may be poled into a polar state by externally applying a high electric field (10-100 kV/cm), usually at elevated

temperatures [14]. After poling, the ferroelectric material exhibits piezoelectric properties, even though the domain polarization directions are simply aligned but not identical.

One of the characteristics of ferroelectric materials is that their polarization-electric field response is non-linear, i.e. it exhibits hysteresis behavior, as a result of the switchable polarization, as shown in figure 2.2 [1]. At low electric field when the field strength is too low to switch unfavorable polarizations (segment AB in figure 2.2), the polarization increases linearly with the magnitude of the electric field. At higher electric field values (segment BC), the field is able to induce polarization switching in favor of the field direction, and the charge density increases drastically with minimal field strength increase. If the electric field is increased to the point where almost all the dipoles are aligned (segment CD), the polarization again starts to increase linearly with the field, at a much slower pace.

If the electric field at this point is decreased, some of the polarizations will switch back, but there is a remnant polarization P_s (E) when field is decreased to zero. To reach zero polarization, the electric field must be reversed to the coercive field - E_c (point F). Further increase of the field in the reverse direction will cause reversed alignment of dipoles and saturation (point G). The field strength is then reduced to zero and reversed to complete the cycle [1].

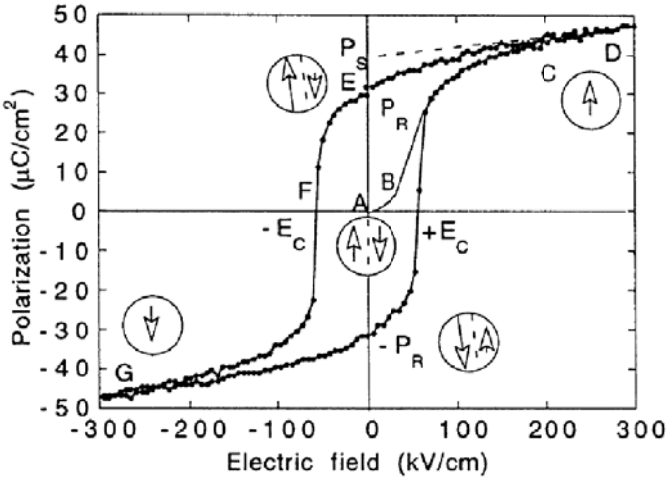


Figure 2.2 Hysteresis loop of $PbZr_{0.45}Ti_{0.55}O_3$ thick film [14]

For PZT compositions that are Zr rich, the material starts to exhibit antiferroelectric behavior; addition of Lanthanum can further stabilize the antiferroelectric phase. The antiferroelectric material has dipoles that are antiparallel, which transfers to ferroelectrics under an applied electric field. Therefore, the antiparallel configuration delays the ferroelectric behavior, resulting in two hysteresis loops instead of one. A typical double hysteresis loop for antiferroelectric materials is shown in figure 2.3 [15].

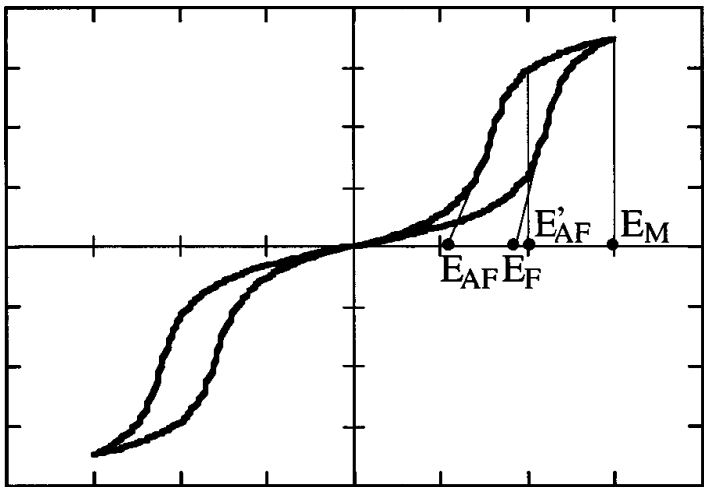


Figure 2.3 Typical double hysteresis loop for antiferroelectric materials [15]

2.1.1.4 Piezoelectric Properties

(1) Definition

The piezoelectric effect is defined as the appearance of an electric potential across certain faces of a crystal when it is subjected to mechanical pressure. The effect is the result of the ionic displacement in crystals that have a non-centrosymmetric structure. When the crystal is subjected to strain, the ions are displaced such that the center of positive charges does not overlap with the center of negative charges, causing the electric polarization of the crystal. This is the direct piezoelectric effect.

On the other hand, when an external electric field is applied to the crystal, the ions are displaced by electrostatic interactions, resulting in mechanical strain of the crystal. This is the converse piezoelectric effect.

(2) Figure of Merits

For the piezoelectric effect, the relationship between the applied stress X_{jk} and the charge density measured D_i is

$$D_i = d_{ijk} X_{jk}$$

where d_{ijk} is a third rank tensor of piezoelectric coefficients [1].

For the converse piezoelectric effect, the relationship between the applied electric field E_k and the developed stress x_{ij} is

$$x_{ij} = d_{kij} E_k$$

where d_{kij} is a third rank tensor of converse piezoelectric coefficients and identical to the direct piezoelectric coefficients [1]. According to crystal symmetry, the number of piezoelectric coefficients can be reduced. Two commonly used piezoelectric coefficients are d_{33} when the electric field and strain are in the same direction, and d_{31} when the electric field is normal to the strain direction.

Another figure of merit for piezoelectric materials is the electromechanical coupling factor k_p. It is defined as

$$k^2 = \frac{\text{Stored electrical energy}}{\text{Input mechanical energy}}$$

for the direct piezoelectric effect, and

$$k^2 = \frac{\text{Stored mechanical energy}}{\text{Input electrical energy}}$$

for the converse piezoelectric effect.

(3) Piezoelectric properties of PZT and PLZT

In addition to electric field, PZT and PLZT can also be polarized by mechanical stress (direct piezoelectric effect), and strain can be induced in the material by electric field (converse piezoelectric effect), thus rendering it an ideal piezoelectric material. In fact, polarization switching by an external electric field in ferroelectric materials can lead to strain–electric field hysteresis, as shown in figure 2.4 [1], which is unique for ferroelectric materials. The butterfly-shaped curve is due to (1) the normal converse piezoelectric effect of the lattice, and (2) switching and movement of domain walls [1].

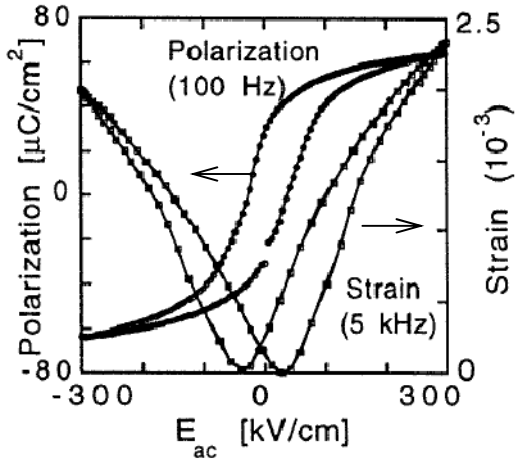


Figure 2.4 Strain-electric field relationship and hysteresis loop for PZT [1]

2.1.1.5 Composition-property Relationship

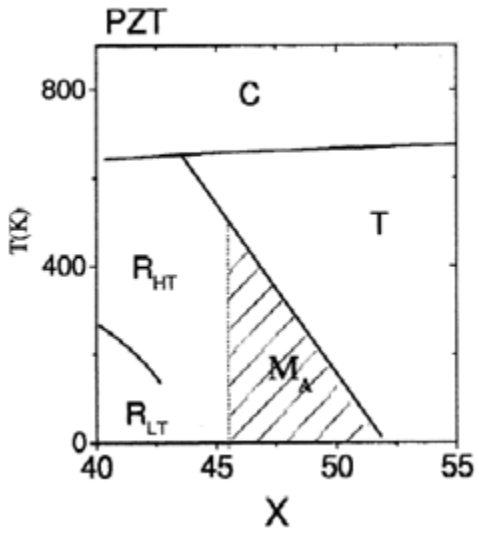


Figure 2.5 Phase diagram of PZT [16]

The phase diagram of PZT is shown in figure 2.5 [16], in which the X axis denotes percentage of $PbTiO_3$. Above the Curie temperature (region C in figure 2.5), only highly symmetric cubic phase may be present. At lower temperatures, however, there are two phases of lower symmetry possible: rhombohedral (R_{HT}) and tetragonal (T). The most remarkable properties arise when the compositions are near X=50%, or more specifically, $PbZr_{0.53}Ti_{0.47}O_3$ at room temperature. This composition sits right at the boundary separating the tetragonal and rhombohedral phases, known as the morphotropic phase boundary (MPB), and thus the two phases can coexist. It has been recently found that a monoclinic phase in the vicinity of the MPB is possible, making the material "softer" and result in higher piezoelectric properties [16].

Figures 2.6(a) and (b) show the variation of piezoelectric coefficient, dielectric permittivity and electromechanical coupling factor as a function of composition [1]. Near

the MPB, the dielectric properties as well as piezoelectric properties reach their peaks. These compositions are therefore highly sought after for both applications.

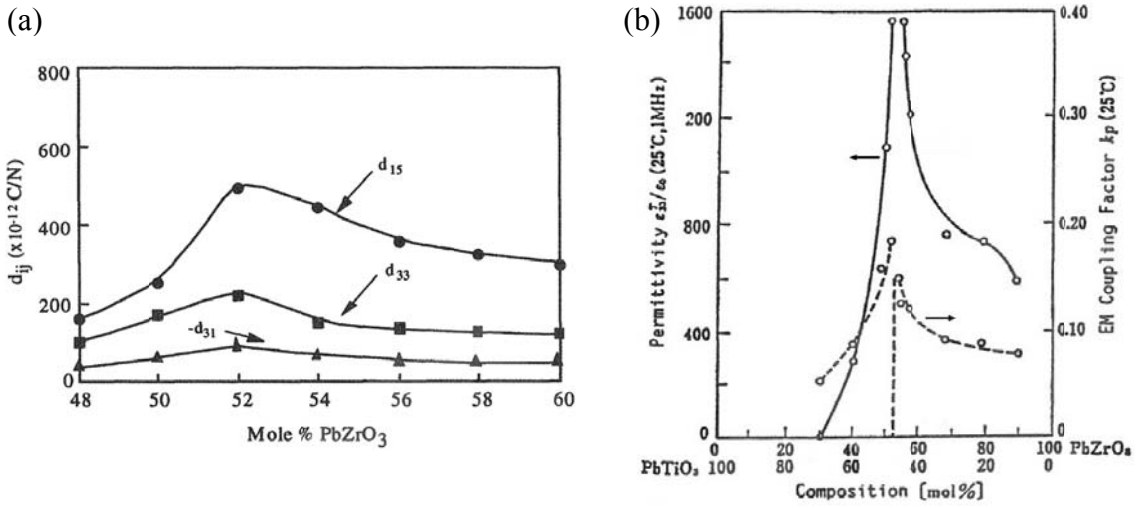


Figure 2.6 (a) Variation of piezoelectric constant with composition of PZT (b) Variation of permittivity and electromechanical coupling factor with composition of PZT [1]

2.1.2 Synthesis Methods

2.1.2.1 Physical Vapor Deposition

RF Sputtering

In RF sputtering, energetic charged ions are accelerated towards the target material which is also the film forming material. The ion bombardment causes the target atoms to fly off the target surface and deposit on the substrate. RF sputtering is a widely used method for PZT thin film deposition. Due to the high crystallization temperatures of the PZT ceramics, as-deposited films are usually amorphous and need post-sintering at elevated temperatures. However, the process offers poor uniformity over large area, poor control of the stoichiometry, and very poor step coverage on 3-D surfaces. The latter is one of the most critical properties required for ULSI integration and MEMS device fabrication.

Pulsed Laser Deposition (PLD)

The equipment for pulsed laser deposition (PLD) consists of the excimer laser, optics and deposition chamber. Typically, the laser goes through the focusing lens and is focused on the rotating target within the chamber at 45˚ incident angle; the ablated materials are deposited on the substrate which is facing the target, at a distance of several millimeters. A typical PLD set-up is illustrated in figure 2.7 [17].

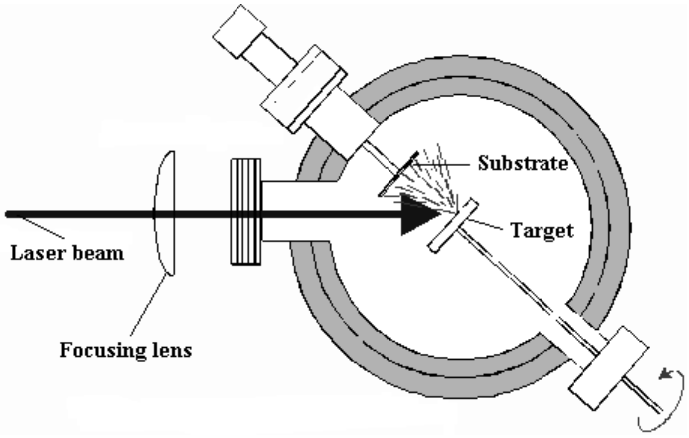


Figure 2.7 Configuration of PLD equipment [17]

PLD is known to deposit thin films via particulate ejection of the ablated material and a good way to keep the target composition due to instantaneous melting under extreme high temperatures produced by the laser. The background gas pressure, substrate-to-target distance, laser energy and wavelength are all critical parameters that can affect the film quality [18]. PZT thin films can be readily obtained with non-epitaxial substrates; and with single crystal MgO or $SrTiO_3$ as substrate, epitaxial PZT thin films with Zr content of 0-0.6 can be deposited by PLD [19]. However, similar to sputtering, PLD offers very poor step coverage on 3-D surfaces, limiting its application in many fields.

2.1.2.2 Chemical Vapor Deposition

Metallorganic Chemical Vapor Deposition (MOCVD)

In MOCVD, the metallorganic chemical precursors are vaporized into their gaseous phase and are transported into a reaction chamber via a chemically inert carrier gas. These molecules are adsorbed on the substrate and subsequently undergo a chemical reaction resulting in the formation of thin films. The reaction byproducts are carried away from the growing film by the carrier gas. A schematic illustration of MOCVD equipment is shown in figure 2.8 [20].

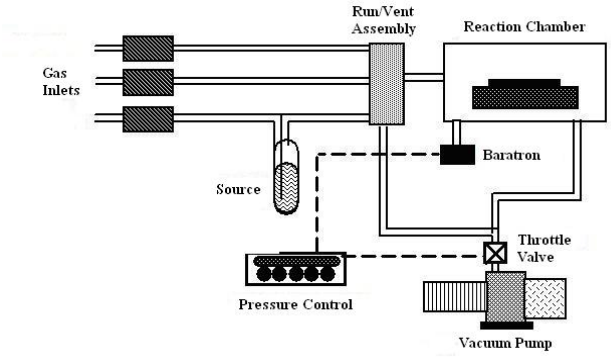


Figure 2.8 MOCVD equipment [20]

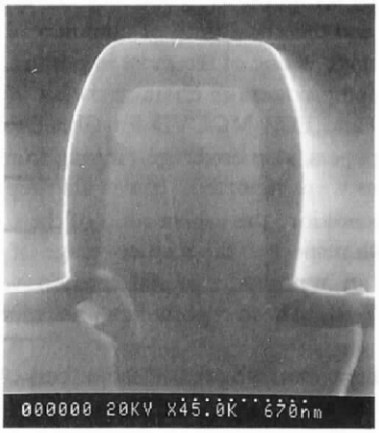


Figure 2.9 Morphology of MOCVD PZT film on a Si trench of aspect ratio 1.1 [21]

As a commercially established and well-studied fabrication technique, MOCVD offers good stoichiometry control, high film densities, high deposition rates, high conformality

over large areas and excellent step coverage. Figure 2.9 shows an SEM image of MOCVD PZT on Si trenches of aspect ratio 1.1, from the study of Shimizu *et al*. [21]. The step coverage is reported to be 75%. It is obvious that the conformality of this method is still not good enough and would be even worse with higher aspect ratios.

2.1.2.3 Chemical Solution Deposition (CSD)

Precursor Solution Preparation

According to the different solution chemistry, CSD can be divided into three categories:

(1) Sol-gel processes

(2) Chelate processes that use modifying ligands

(3) Metallorganic decomposition (MOD) routes

(1) Sol-gel process

The sol-gel process for PZT synthesis usually utilizes 2-methoxyethanol (CH_3-OCH_2CH_2OH), or 2-ME for short, as the solvent and alkoxides as the solute. In this case, the starting reactant is very active and the reaction temperature is relatively high, and in the process the reactants go through hydrolysis to form networks and partial condensation [22]:

Hydrolysis:

$$M(OR)_x + H_2O \rightarrow M(OR)_{x-1}(OH) + ROH$$

Condensation (alcohol elimination):

$$2M(OR)_{x-1}(OH) \rightarrow M_2O(OR)_{2x-3}(OH) + ROH$$

Condensation (water elimination):

$$2M(OR)_{x-1}(OH) \rightarrow M_2O(OR)_{2x-2} + H_2O$$

(2) Chelate Process

The chelate process is a synthesis route that also utilizes alkoxides as starting reactants for the B-site species, but mostly relies on the molecular modification of the alkoxides compounds. Common chelating agents include acetic acid and acetylacetone. Hydrolysis and condensation still takes place in this case, but the most important reaction in this case is the chelation of the metal alkoxides [22]:

$$M(OR)_n + x\ CH_3COOH \rightarrow M(OR)_{n-x}(OOCCH_3)_x + x\ ROH$$

Chelating agents serve to depress the moisture sensitivity of the alkoxides, increasing the shelf life, and distillation and refluxing is not needed in the solution preparation. They also modify the molecular structure of the reactant and can greatly influence the resulting structure and properties of resulting species. Pyrolysis behavior, for instance, will change dramatically with the addition of chelating agents. Chelating agents also make the chemical reactions during the solution preparation more complex and less controllable, and the solution changes more drastically with stock time. However, high quality PZT thin films can still be achieved with this method.

(3) Metallorganic Decomposition Process (MOD)

The MOD process employs carboxylate compounds, which are not water-sensitive [22]. The process is usually extremely simple, which is, basically, intermixing of the starting compounds according to stoichiometry in a common solvent (usually xylene). Since the starting compounds are not water-sensitive, oligomerization does not take place and the starting compounds basically retain their original structure in the solution.

Although the process is simple in the MOD solution synthesis, the large organic ligands of the starting reactant often results in large shrinkage during the subsequent thin film deposition process which often leads to cracking. Therefore the control of the heat processing and the solution concentrations are more important. Control of film properties and microstructure is also harder compared to sol-gel and chelate routes due to the

relatively low reactivity of the starting compounds and the lack of chemical modification capabilities.

Thin Film Deposition from the Solution

The synthesized precursor solution is often deposited on a substrate by regular spin coating or dip coating, though some processes require filtering of the solution prior to that to eliminate precipitates. The as-deposited film is amorphous and highly porous, with a significant amount of organic ligands embedded. The film properties highly depend on the precursor and the solvent at this stage.

Low Temperature Heat Treatment/Drying

After the film deposition process, the film is often put through a low temperature annealing step in order for pyrolysis to take place, usually under environmental or oxygen enriched atmosphere. In this way, the organic components are eliminated before the gel network collapses, which result in better electrical properties of the film.

An alternative is to perform the pyrolysis step together with the final high temperature annealing, resulting in one-step annealing [22]. The claimed advantage of this method is that the film quality will be improved due to delayed onset of crystallization and thus, the film will go through the crystallization at a higher temperature than normal. Although the temperature ramp rate is usually considerably high in this case, film cracking is unlikely to occur due to the flexible structure of the gel network at the time high temperature is applied.

High Temperature Heat Treatment/Sintering/Annealing

PZT crystallization takes place at around 550 ℃ [23]. Typical high temperature annealing heat treats the thin film at temperatures 500-800℃ to ensure good quality

films. The heat treatment can be done in either a low ramp rate, high thermal budget way with traditional furnaces, or in a very high ramp rate with rapid thermal processing (RTP) furnaces. The benefits of using RTP are that, first, the rapid ramp rate allows for later onset of crystallization and higher crystallization temperatures, thus higher quality crystals; secondly, the small overall heat budget and short treatment time can suppress some processes (such as undesirable diffusion) kinetically. Considering the unique characteristics of PZT, however, there are several other considerations to take into account when designing this crystallization step.

The problems during crystallization mostly come from the lead component. Lead oxide is highly volatile at elevated temperatures and often escapes from the thin film, leaving the composition inhomogeneous and nonstoichiometric. The resulting film is often off the target stoichiometry, or even crystallized into the pyrochlore phase, which is the intermediate phase when amorphous PZT transforms to perovskite [24].

In some cases, such as near the morphotropic phase boundary, these problems can be easily remedied by adding excess amount of lead precursor in the precursor solution. The amount of excess lead needed is dependent on the heat treatment, but usually in the 5-10 mol% range. For PZT compositions that are Zr rich, however, even excessive lead up to 25% still would not result in phase-pure thin films. In this case, the PZT crystallization is much slower than for Ti rich compositions, and it is very difficult to compensate the lead loss just by excess starting precursors. A more effective method is to employ a PbO overcoat on top of the film, which has been proven to be able to produce phase-pure PZT films that are Zr rich [25].

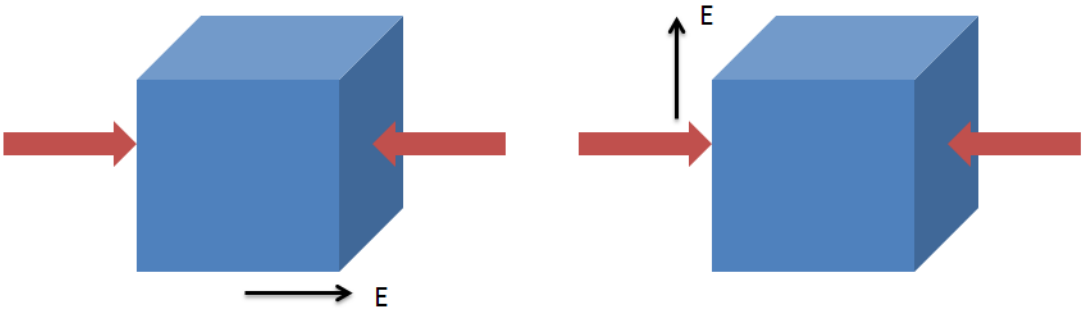
2.1.2.4 Hydrothermal Synthesis

The hydrothermal process is a direct growth process from the solution phase, rather than a solution deposition technique. The preparation of PZT thin films using hydrothermal method is first reported by initially using reactions between the TiO_2 substrate and solutions containing lead and zirconium to form PZT or PZ nuclei on the surface, followed by a second reaction step using solutions containing lead, titanium and zirconium [26]. The method has been modified and optimized since then, but the resulting film has a rough texture and usually has a lot of hydroxyl groups incorporated, which results in poor electrical properties overall, though its piezoelectric properties can rival that of the bulk.

2.1.3 Applications of PZT Thin Films

2.1.3.1 Microelectromechanical Systems (MEMS)

As the standard material with high piezoelectric coefficient, PZT has been widely used in MEMS devices such as piezoelectric MEMS actuators [27], sensors [28], and power generators [8]. Here we emphasize the power generator application.



(a) (b)

Figure 2.10 Two working modes for piezoelectric energy generation: (a) d_{33} mode, (b) d_{31} mode

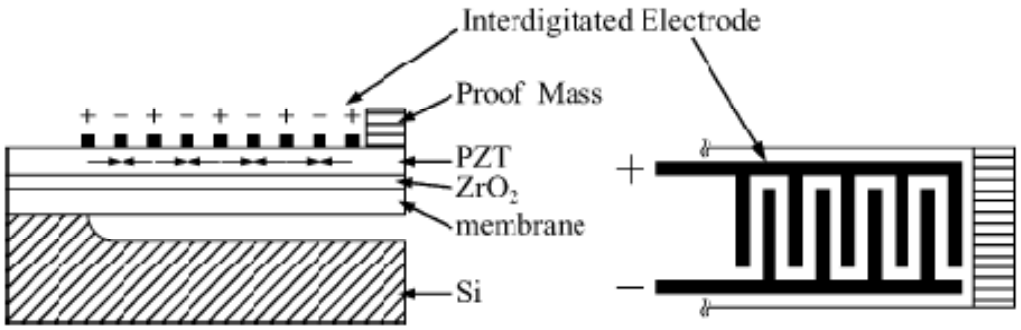
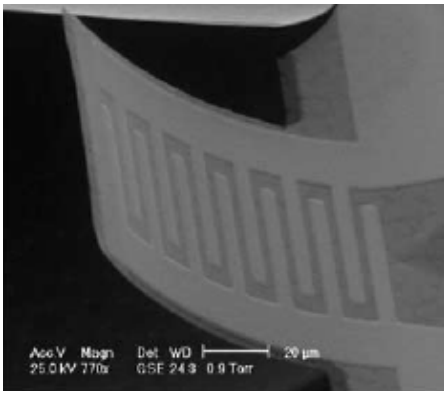


Figure 2.11 Design of the d_{33} mode PZT MEMS generator [8]

(a)



(b)

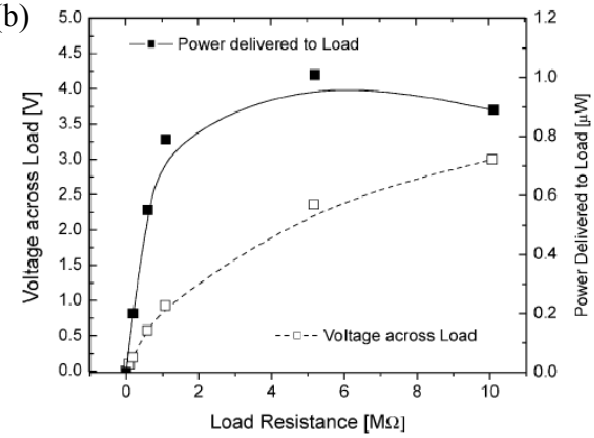


Figure 2.12 (a) SEM image and (b) output of the d_{33} mode PZT MEMS generator [8]

Several designs for MEMS power generator have been demonstrated, and most are based on bimorph structures on a freestanding Si cantilever utilizing the d_{31} mode, which is 2-3 times lower than d_{33}. An illustration of the two working modes is shown in figure 2.10. A design of power generator that operates on d_{33} mode has been proposed by Y. B. Jeon *et al*., and the device structure is shown in figure 2.11 [8]. PZT thin films of 480 nm were fabricated by a sol-gel spin-on method and subsequently poled. The d_{33} work mode is achieved by utilizing interdigitated electrodes. The MEMS generator is mechanically actuated at a frequency of 13.9 kHz which is the lowest resonant frequency of the cantilever. The charge is then rectified and stored to power the load. Figure 2.12 (a) is the

SEM image of the device, and (b) shows the power output of this device, with the maximum output voltage being 3V and power being 1μW.

2.1.3.2 Ferroelectric Capacitors and Memory

Ferroelectrics are widely used for capacitor applications due to their high dielectric constant. One noteworthy application is in decoupling capacitors which decouples the load from the power source, enabling the smooth operations of the load despite unstable power. For this type of applications, the integration of the ferroelectrics with the other electronic component is a limiting factor, and though direct fabrication on PCB is not possible, post-process integration can be done by lamination [29].

Ferroelectrics have also been widely researched for ferroelectric random access memory (FeRAM) applications. In FeRAMs, the remnant polarization in ferroelectric capacitors is switched and sensed as the storage unit. FeRAM offers the distinct capabilities such as high endurance data storage, fast write data protection, and extended battery life, and is one of the most mature non-volatile memory technologies today [30]. PZT used for FeRAMs are mostly high quality, ultrathin films deposited by MOCVD, and besides superior electrical properties, fatigue and retention should all be taken into account for memory applications.

2.2 Fabrication and Characterization of PZT/PLZT Thin Film Devices

2.2.1 Silicon Dioxide Barrier Layer Deposition

A 500 nm SiO_2 layer was deposited on commercial 4□ Si wafers using Plasma Enhanced Chemical Vapor Depositor (PECVD) in a cleanroom environment. The silicon dioxide layer acts as a buffer layer to prevent metal diffusion into Si.

Inside the PECVD chamber, SiH_4 and N_2O were supplied and chemically react in RF induced plasma to deposit SiO_2 at an RF frequency of 13.56 MHz. The chamber temperature was set at 250℃, and the flow rate for SiH_4 and N_2O was set at 900 sccm (standard cubic centimeters per minute) for each. At the power of 25 W, the deposition rate of SiO_2 was measured to be approximately 500 A/min. Therefore a 10 min deposition yields a total thickness of 500 nm.

2.2.2 Bottom Electrode Deposition

To enhance the smoothness of the substrate and good adhesion with subsequent deposited layers, prior to any electrode material deposition, the oxidized wafers were cleaved into 4 pieces, washed with DI water, then with acetone, isopropanol and ethanol to eliminate any organic contaminates, before final DI water wash. The wafers were then dried with blowing nitrogen and baked on a hotplate at 120℃ for ten minutes to eliminate moisture. All processes are done in a cleanroom environment.

2.2.2.1 Metal Electrode Sputtering

Pt is a well-established electrode material for PZT due to its chemical stability and thus lack of interaction with either the overlying oxide film or the oxygen in the atmosphere during the high temperature process steps.

Although Pt electrodes are widely accepted as the standard electrode for PZT, one intrinsic drawback of the material is that it cannot be electroplated, making it impossible to cover surfaces with complex morphologies. Therefore, it is highly desirable to investigate the process compatibility of PZT with metals that are electroplating compatible. Of all metals that can be deposited by electroplating, Ni is the most stable in elevated temperatures, and therefore it was chosen as one of the candidate electrode materials in this study.

For metal electrode deposition, a DC sputtering system in a cleanroom environment was utilized. First the chamber was pumped to a base pressure of 2×10^{-5} Torr; then the chamber was filled with Argon to a pressure of 6mT for sputtering. To enhance adhesion to the Si wafer surface and prevent Si outdiffusion during subsequent high temperature processes, a 3'' Ta (99.95%) target was used to produce Ta barrier layer of thickness 30nm. A 500nm Pt or Ni thin film was then deposited with 3'' Pt or Ni target without breaking the vacuum as the electrode.

2.2.2.2 $LaNiO_3$ Sol-gel Electrode Preparation

To realize PZT applications where three-dimensional structure is preferred, it is necessary to develop electrodes that can be conformally coated on a non-planar surface on the micro-scale, such as etched silicon trenches.

Similar to PZT, $LaNiO_3$ has the perovskite structure and also presents high conductivity, and is a promising material as both electrode and lattice-matched buffer layer for PZT. A sol-gel approach to synthesize $LaNiO_3$ was taken to evaluate its possibility to be coated on a 3-D surface conformally.

To remove water content, Lanthanum(III) nitrate hexahydrate ($La(NO_3)_3 \cdot 6H_2O$, 99.99%, Sigma Aldrich) and Nickel(II) nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$, 98.5%, Sigma Aldrich) were dehydrated separately. The crystals were first dissolved in 2-methoxyethanol (2-ME), and then the solvent was evaporated under vacuum with warm water bath of 60-80℃ until the remains became dry powders of the reactant. The process was then repeated three times. Care had been taken so that the exposure to air is minimized to suppress moisture re-adsorption.

The dehydrated $La(NO_3)_3$ powder was then transferred to a glovebox filled with Argon, in which an appropriate amount of 2-ME was added. The mixture was then transferred to a reflux set-up under Argon environment with constant stirring for 4-6 hours. Oil bath was employed to maintain the refluxing temperature of 125 ℃, which is the boiling point of the solvent. Subsequently, dehydrated $Ni(NO_3)_2$ powder was added with the molar ratio of 1:1 and an appropriate amount of 2-ME was replenished in a glovebox environment to achieve the concentration of 0.5 mol/L. The solution is then refluxed for another 4-6 hours to ensure homogeneity. The process flow is shown in figure 2.13.

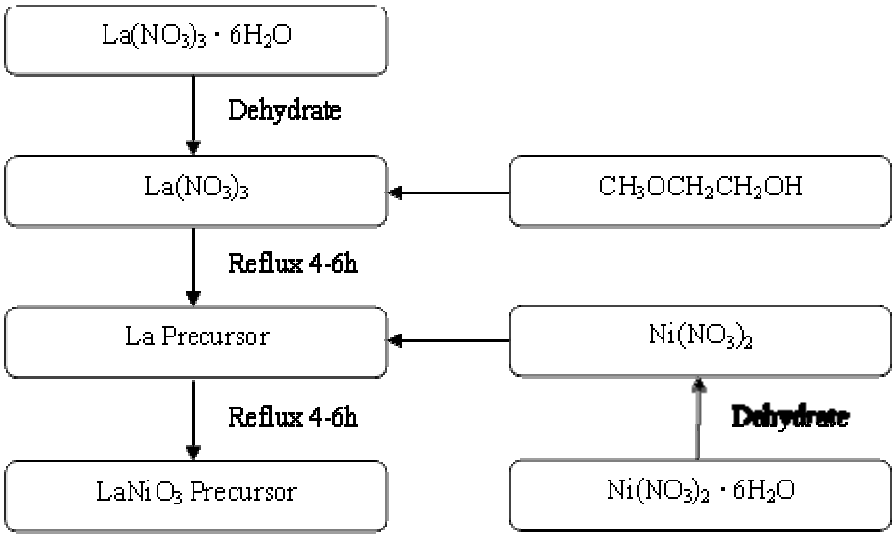


Figure 2.13 Process flow for $LaNiO_3$ sol preparation

The reflux set-up is illustrated in figure 2.14 [31].

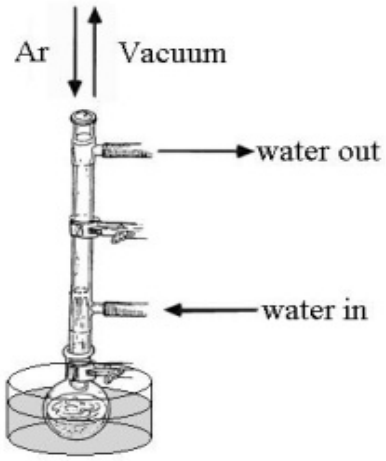


Figure 2.14 Reflux set-up [31]

The finished solution was then spin-coated on the cleaned wafers in a cleanroom environment, with 3000 rpm for 30s. The gel film was then dried on a hotplate at 120 ℃ for 300 s. Then a pyrolysis heat treatment at 400 ℃ for 600 s in air was done to partially burn out the organic content in the dried gel film. The spin-coat and drying process is repeated several times to acquire the desired thickness.

The thin film is then annealed in either a regular tube furnace in air or oxygen at 500 - 600℃ for 1 hour or in an RTP furnace at 600℃ for 1 min in oxygen.

2.2.3 PZT and PLZT Thin Film Preparation

2.2.3.1 PZT and PLZT Sol Preparation

Preparation of the sol from multiple precursors in organic solvent is the most critical part of the entire processing as precursors are sensitive to humidity and atmospheric exposure. To prepare PZT sol-gel solution, Lead(II) acetate trihydrate ($Pb(CH_3COO)_2 \cdot 3H_2O$, Aldrich, 99.999%) was dehydrated for three times using the method described in section 2.2. The dried powder was then transferred into a glovebox and an appropriate amount of 2-ME is added. The solution was then refluxed at 120℃ for 6 hours in Argon

environment. Titanium isopropoxide ($Ti[OCH(CH_3)_2]_4$, Sigma-Aldrich, 99.999%) and Zirconium n-propoxide ($Zr(OCH_2CH_2CH_3)_4$, Alpha, 70% in n-propanol) were then added separately in a similar manner, with refluxing time of 4 hours after each addition. Several compositions have been studied from $PbZr_{0.53}Ti_{0.47}O_3$ to $PbZr_{0.95}Ti_{0.05}O_3$. $Pb_{0.92}La_{0.08}(Zr_{0.95}Ti_{0.05})O_3$ (PLZT) thin film is fabricated by an additional step in which $La(NO_3)_3$ is added into the precursor after dehydration. To suppress harmful phase formation due to lead oxide evaporation, 15% excess lead in molar ratio is used for all compositions. The process flow for PZT and PLZT sol is illustrated in Figure 2.15.

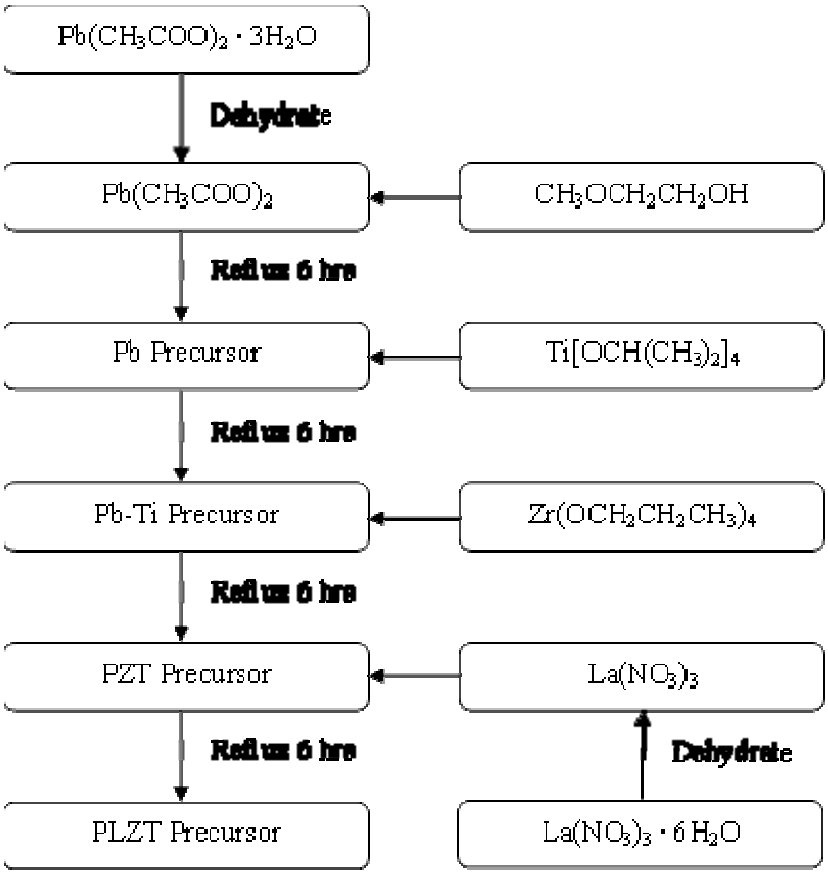


Figure 2.15 Process flow for PZT and PLZT sol preparation

2.2.3.2 Spin Coating of the Sol

The finished solution is spin-coated on the cleaned wafers in a cleanroom environment, with 3000 rpm for 30 s. The gel film is then dried on a hotplate at 120℃ for 300s. Then a pyrolysis heat treatment at 400 ℃ for 300 s in air is done to partially burn out the organic content in the dried gel film. The spin-coat and drying process is then repeated 4 times to acquire the desired thickness.

Due to the phase instability for high Zr content, three approaches have been tried to produce composition graded thin films: (1) using one coating layer of PZT on top of four coatings of PLZT as capping layer; (2) using one coating layer of PZT at the bottom of four coatings of PLZT as buffer layer, and (3) using one coating layer of PZT both on top and at the bottom of three coatings of PLZT to sandwich the unstable compositions.

2.2.3.3 Heat Treatment

After the thin film coating is finished, the wafer was then pyrolyzed in RTP at 420℃ in oxygen for 90 s, and crystallized at 700 ℃ in air for 30 s.

2.2.4 Top Electrode Deposition

Gold films of 300 nm thick were deposited on the PZT/PLZT through a shadow mask with a CVC e-beam evaporator. The chamber was evacuated to 2×10^{-6} - 5×10^{-7} Torr prior to gold deposition.

Three types of shadow mask were used:

Device type I: Round top electrode with diameter 0.6mm. Total area is 0.28mm^2.

Device type II: Rectangular electrode with the size of 1.18mm×2.5mm. Total area is 2.95 mm^2.

Device type III: Rectangular electrode with the size of 2.87×2.5mm. Total area is 7.18 mm^2.

Evaporation technique, rather than sputtering techniques, was chosen for its line-of-sight deposition and poor step coverage. The shadow mask gives clear-cut boundaries, rendering the area of the device well-defined.

The structure of the finished device is illustrated in figure 2.16 (not to scale).

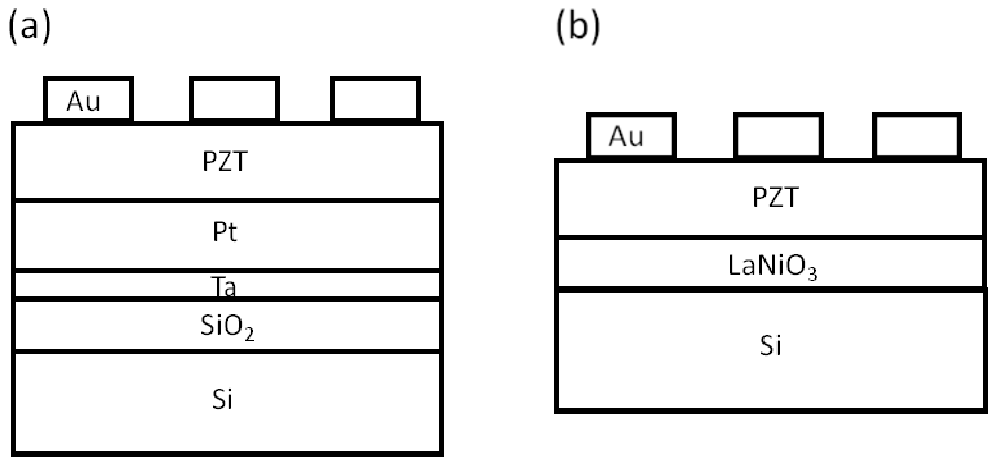


Figure 2.16 Device structure for PZT with (a) Pt electrode and (b) $LaNiO_3$ electrode

2.2.5 Conformal Coating of Sol on 3-D Surfaces

To demonstrate the capability to coat three-dimensional structures conformally with sol-gel process, the as prepared solution was coated on the surface of etched Si trench.

Two types of Si trenches were used in this study:

Trench Type I: Etched by ICP from a mask with dot patterns. The opening is around 30 μm in diameter and has an aspect ratio of around 7, with an inter-opening distance of 30 μm. The opening is etched through the thickness of the Si making it open-ended. The geometry is as illustrated in figure 2.17 (a).

Trench Type II: Etched by ICP from a mask with line patterns. Some of the trenches are of the dimension of around 30 μm in width and 200 μm in height, resulting in an aspect ratio of 7. And some are 3 μm in width and 200 μm in height. The pattern is in 5mm×5mm squares and repeat throughout the whole wafer. The geometry is as illustrated in figure 2.17 (b).

Type I and type II trenches have the same feature size and aspect ratio, and though their geometric configuration is different, their surface areas are almost the same.

The desired trench morphology after an ideal conformal coating is illustrated in figure 2.17 (c) and (d) for two different types, respectively.

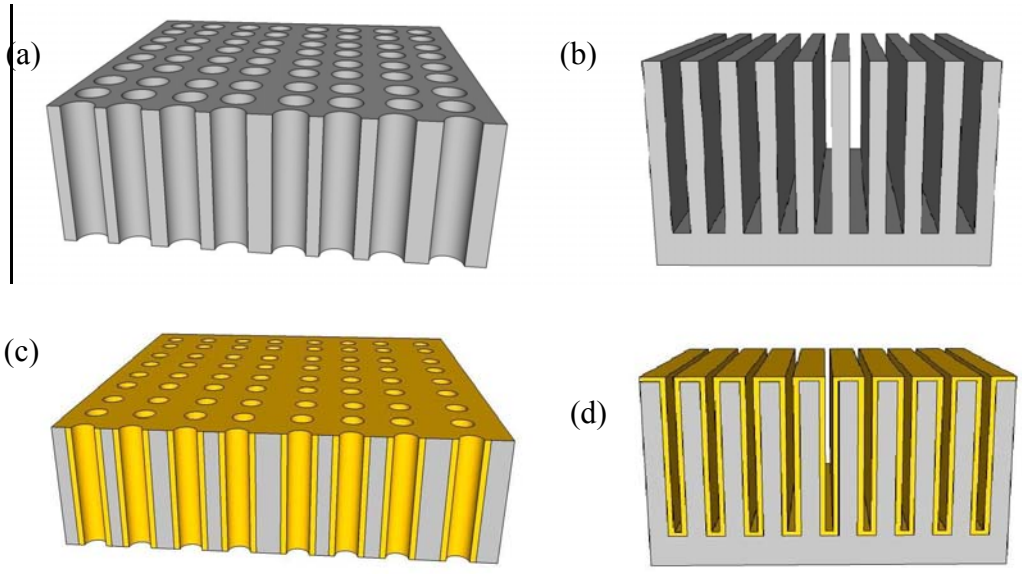


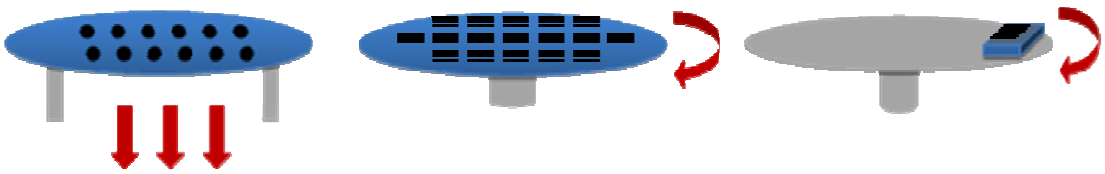
Figure 2.17 Illustrations of trench coatings: (a) geometry of trench type I (b) geometry of trench type II (c) the desired coating on trench type I, and (d) the desired coating on trench type II

Three methods were employed and evaluated in order to coat the trench surface conformally:

(1) For trench type I, vacuum assisted infiltration was used in which the etched Si wafer was placed on a platform such that the trench direction is vertical, with the edge of the wafer sealed. The sol was then dispensed onto the wafer surface. Vacuum was immediately applied from underneath the wafer to infiltrate the sol into the trench. The setup is illustrated in figure 2.18 (a). The coating was then dried, after which spin-coating was repeated for one time and then pyrolyzed and crystallized as in the planar process.

(2) For trench type II, direct spin coating was used in which the etched Si wafer is placed on the spinner such that the trench direction is horizontal. The sol was then dispensed onto the wafer surface. Spin coating was then performed in a regular manner. The setup is illustrated in figure 2.18 (b). The sol was dispensed on the trenches and then spun at 3000 rpm for 30 s, and subsequently dried. The coating was then dried, after which spin-coating was repeated for one time and then pyrolyzed and crystallized as in the planar process.

(3) For trench type II, radial direction spin coating was used in which the Si wafer was diced into squares with one set of trench patterns on each. The diced Si wafer piece was then fixed on the edge of a round carrier plate such that the direction of the line pattern was the radial direction of the plate, and the whole plate was put in a conventional spin coater. The setup was illustrated in figure 2.18 (c). The sol was dispensed on the trenches and then spun at 3000 rpm for 30 s, and subsequently dried. The coating was then dried, after which spin-coating was repeated for one time and then pyrolyzed and crystallized as in the planar process.



(a) (b) (c)

Figure 2.18 Illustrations of coating set-up: (a) vacuum assisted infiltration (b) direct spin coating (c) radial direction spin coating

2.2.6 Device Characterization

2.2.6.1 Optical Microscope Observations

To determine if the synthesized films are crack free over a large area, optical microscope characterization was used. Since the target of observation is on a large scale (typically in mm), a 5X magnification was used.

2.2.6.2 Profilometry Measurement

Sputtered metal electrode thickness, sol-gel $LaNiO_3$ and PZT thickness are measured with a Tencor KLA profilometer. During film deposition, some area of the substrate is protected by Kapton tape, which is later removed to form a step with the deposited area. The profilometer stylus is then programmed to measure the step height. To yield accurate film thickness, more than three measurements are made on the same film to give an average thickness value.

2.2.6.3 Four-Point Probe Measurement

The resistivity of the sol-gel $LaNiO_3$ thin film was characterized with a Signatone four-point probe. The probe station is first calibrated with a standard sample. The measured film thickness is input into the program to calculate the resistivity from I-V measurement. Fixing the calibration constant, the measuring current is increased step-by-step until the

reading is constant to the 4th digit. The final reading is taken as the resistivity value for the measured thin film.

2.2.6.4 X-ray Diffraction Analysis

X-ray diffraction study of the thin films was done with PANalytical X' pert PRO Alpha Dffractometer. The diffraction profile was measured using Cu-Kα(1.54 Å) radiation and an Xcelerator detector. A divergence slit of ½ degree was employed. A scan rate of 0.002 counts per second was used.

2.2.6.5 Field Emission Scanning Electron Microscope Characterization

Detailed surface morphology and cross-sectional views of the thin films were acquired with FESEM LEO 1530 with resolution of 3nm. The acceleration voltage used was 5kV.

2.2.6.6 Capacitance Measurement

The capacitance and loss measurements of the thin film devices were done using a HP 4285 A Precision LCR Meter (75 kHz – 30 MHz) at 1 Volt and 100 kHz frequency and room temperature. The contacts were made between the exposed bottom electrode layer and the top electrode by a pair of Tungsten probes isolated from gold plated copper shield.

2.2.6.7 DC Leakage Current and Breakdown Voltage (BDV) Measurement

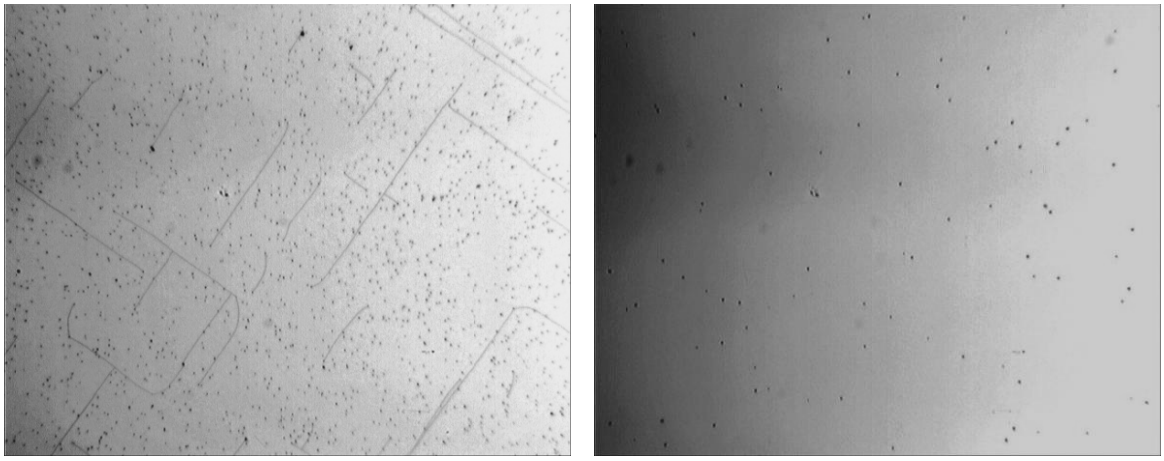
DC leakage current analysis and breakdown voltage (BDV) of the PZT and PLZT devices were measured with a Keithley 236 Source Measure Unit DC analyzer. The equipment is capable of applying a maximum of 110 V with a minimum step size of 1 mV and a maximum current limit of 100mA.

2.3 Results and Discussions

2.3.1 Influence of Process Conditions on Conductivity of $LaNiO_3$ Sol-gel Electrode

2.3.1.1 Effect of Coating Thickness

The 5X magnification optical microscope image of the crystallized $LaNiO_3$ was shown in Figure 2.19. All the films with three coatings, the process yields seriously cracked films with extremely high resistivity due to limited conducting paths. On the other hand, all films made with one and two coatings are crack-free on the micro-scale with reasonable conductivity.



(a) (b)

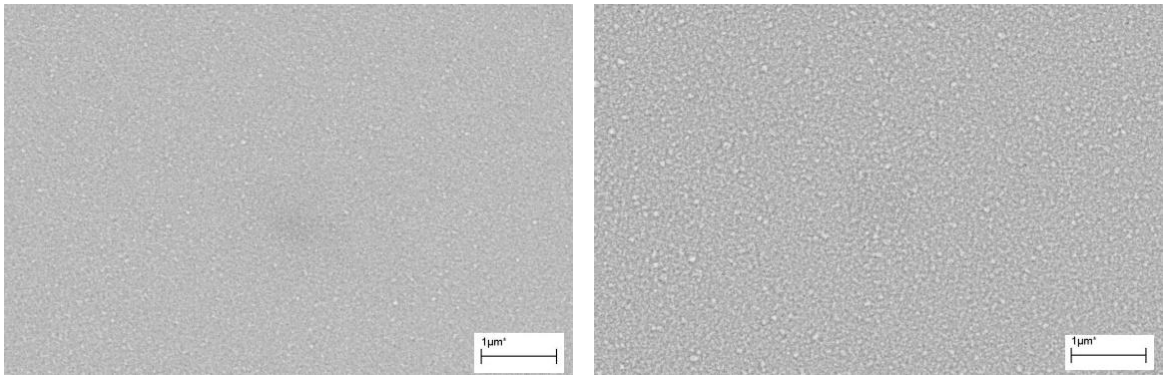
Figure 2.19 Optical image of $LaNiO_3$ thin films on Si with (a) three coatings and (b) two coatings

Thin films are subject to various stresses in the process, from the volume shrinkage of the film itself during drying and crystallization and thermal expansion mismatch with the substrate during heating and cooling. When the thickness of a thin film is above a certain value, known as the critical thickness, stress in the film cannot be relaxed during the process and cracks develop. The critical thickness can be in the range from a few hundred

nanometers to a few microns, depending on the material and the process in question. In this study, the film thickness for each coating of $LaNiO_3$ after crystallization was measured to be around 70 nm. It is therefore inferred that the critical thickness for sol-gel $LaNiO_3$ films is approximately 200 nm. Beyond 200 nm, the films cannot sustain the strain and cracks will develop in a biaxial manner.

2.3.1.2 Effect of Annealing Conditions

Two-coating $LaNiO_3$ thin films of identical processing conditions were crystallized with different annealing conditions. Figure 2.20 shows the SEM image of the derived thin films and it is obvious that furnace annealed sample has a higher degree of crystallization and slightly larger grain size.



(a) (b)

Figure 2.20 SEM image of two-coating $LaNiO_3$ thin films from (a) RTP 600℃ and (b) furnace 600℃ sintering

The resulting resistivity values of the films are summarized in Table 2.1. The resistivity generally falls into the range of 10^{-3} Ohm · cm^{-1} (with the exception of 600℃ anneal in O_2), which is a reasonable value for the application as PZT electrodes. The remarkably higher resistivity after tube furnace annealing in oxygen at 600℃ may be due to oxidation of the underlying Si. For anneal in tube furnace at 500℃, Si is less likely to oxidize and therefore slightly lower resistivity is achieved. The atmosphere doesn't have great

influence on the final resistance at 500℃. Interestingly, a quick anneal with RTP at 600℃ for only one min can achieve the same conductivity level as with tube furnace, with a low thermal budget and less time for interdiffusion of the materials. Even though the film is not highly crystallized as from furnace annealed samples, the obtained conductivity from RTP of this study is comparable to the value obtained on well-crystallized $LaNiO_3$ by Miyake *et al.*[32], while they used higher temperatures (700℃) and longer annealing time. RTP is therefore the preferred method for $LaNiO_3$ electrode annealing in this study.

Table 2.1 Resistivity of $LaNiO_3$ Thin Films Sintered at Different Conditions

Heat Treatment	RTP	Tube Furnace (air)		Tube Furnace (O_2)	
Temperature (℃)	600	500	600	500	600
Time (min)	1	60	60	60	60
Resistivity (Ohm · cm^{-1})	4.43×10^{-3}	1.14×10^{-3}	5.05×10^{-3}	1.45×10^{-3}	6.78×10^{-2}

2.3.2 Properties of PZT Thin Films Fabricated on Metal Substrates

2.3.2.1 Surface Morphology and Crystallinity

Figure 2.21 shows the 5X magnification optical microscope image of PZT thin films of four and five coatings on Pt and Ni electrodes, respectively. Thin films on Pt have smooth surface profiles, while those on Ni are cracked due to the volume expansion when oxidation of the electrode occurs. To prevent Ni oxidation, reduced oxygen partial pressure during annealing or lower temperature and overall heat budget is preferred; however, these conditions will have negative impacts on pyrolysis of the PZT sol as well as the crystallization step. Careful optimization of the conditions was done but Ni oxidation and film cracking cannot be eliminated without greatly compromising PZT

properties. Therefore, conclusions can be drawn that the approach with electroplating-compatible Ni electrode is not feasible. All studies below were done on PZT synthesized on Pt electrodes.

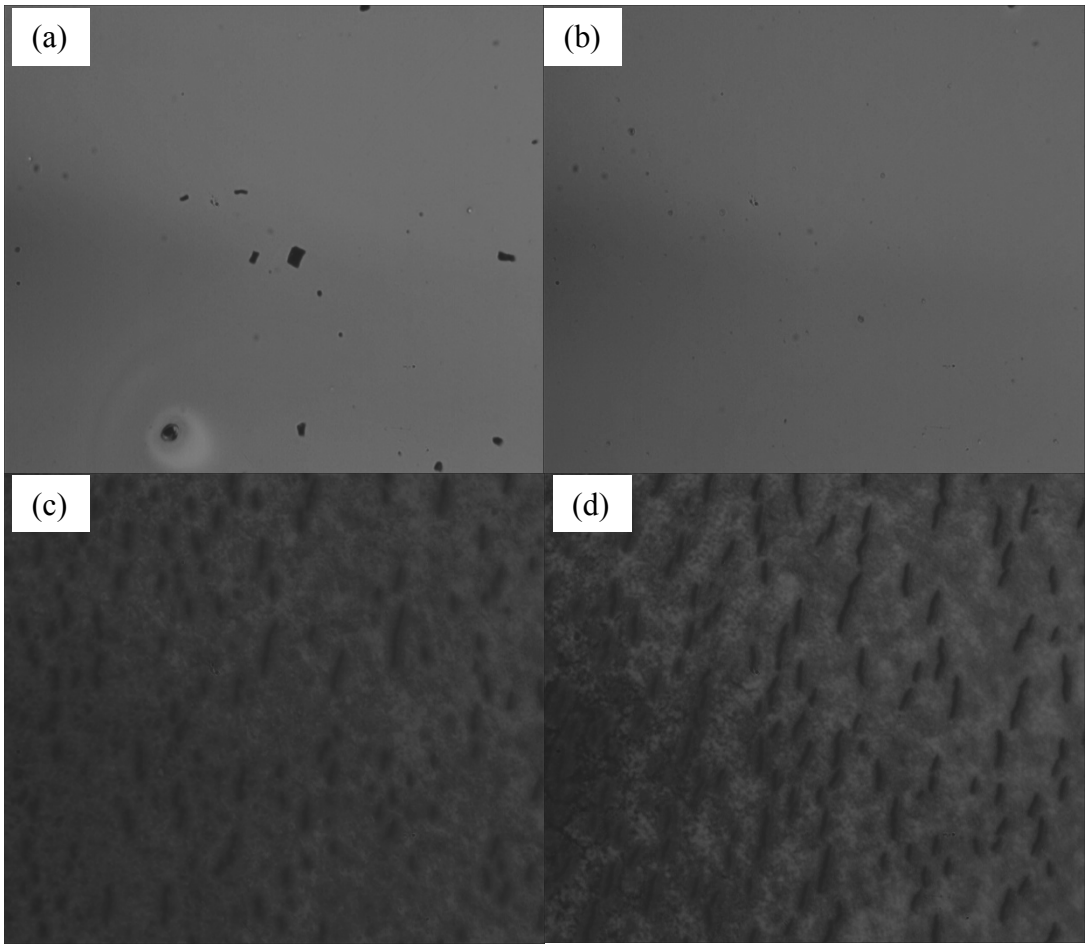


Figure 2.21 Optical images of PZT thin films (a) 4 coatings on Pt (b) 5 coatings on Pt (c) 4 coatings on Ni (d) 5 coatings on Ni

2.3.2.2 Electrical Characterization of PZT Capacitors

The typical values of measured capacitance and other parameters of the capacitor devices on Pt electrode are summarized in table 2.2. Thickness of the film was measured to be 80 nm for one sol-gel coating after sintering. For yield measurement, more than 100 devices of each type were measured. The values were averaged over all working devices from the

same batch of samples, the number of which range from 8-100 depending on the yield. The standard deviation of the measured data is generally less than 10%.

It can be seen that for 320 nm thin films, a capacitance density of 4.48 μF/cm^2 has been achieved with 95% yield on 0.28 mm^2 devices. In comparison, a capacitance density of 4.3 μF/cm^2 was measured on 145 nm sol-gel PZT thin films that are commercially used for Samsung 4Mbit FeRAM devices under 100 kHz [33]. This means that the dielectric constant of the PZT film in this study is 2.3 times of that of the PZT used by Samsung.

Table 2.2 Electrical Properties and Yield of PZT Thin Film Capacitors on Pt at 100kHz, 1V

Thickness (nm)	240			320			400		
Device Area (mm^2)	0.28	2.95	7.18	0.28	2.95	7.18	0.28	2.95	7.18
Capacitance @ 1V (nF)	15.41	/	/	12.54	123.60	/	10.76	93.13	155.94
Capacitance Density @ 1V (μF/cm^2)	5.50	/	/	4.48	4.19	/	3.84	3.16	2.17
Loss	0.103	/	/	0.090	0.307	/	0.076	0.207	0.886
BDV (V)	16.2	/	/	24.2	10.5	/	24.0	16.0	2.8
Leakage @ 3V (μA/cm^2)	0.25	/	/	0.27	0.11	/	0.20	0.11	/
Yield	15%	0%	0%	95%	28%	0%	98%	56%	14%

(1) Effect of Film Thickness on Device Capacitance and Yield

The capacitance value of a parallel capacitor is calculated by

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

In which ε_0 and ε_r are permittivity of vacuum and relative permittivity of the dielectric material, respectively; A is the plate area, and d is the inter-distance of the two plates, i.e. the film thickness. Therefore, the capacitance of a parallel plate capacitor should scale with the area and decrease with increasing film thickness. Figure 2.22 shows the capacitance density and loss tangent as a function of PZT thickness. Both of the two parameters show an inverse linear relationship with thickness.

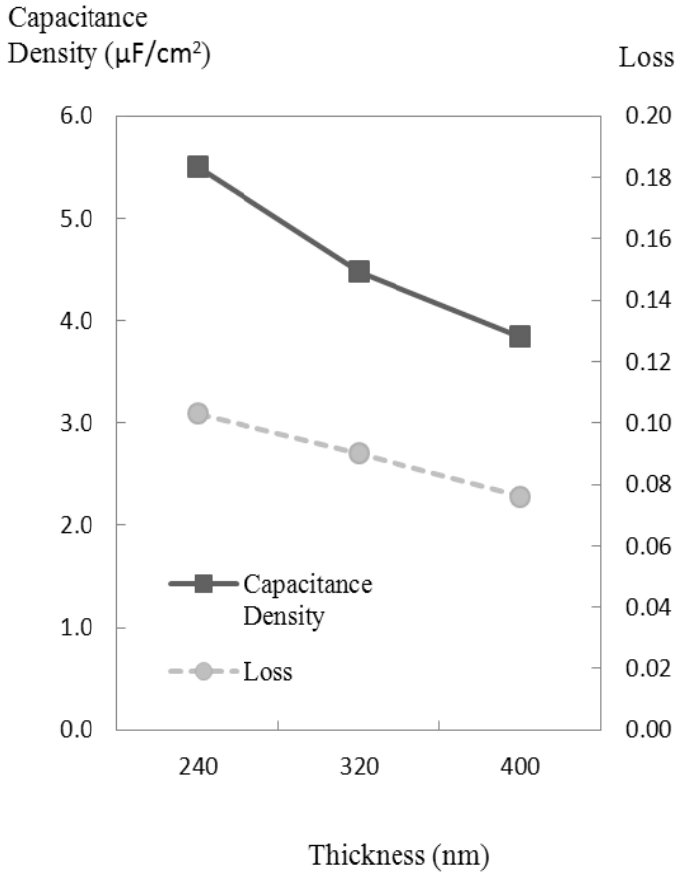


Figure 2.22 Effect of film thickness on PZT capacitance and loss at 100 kHz

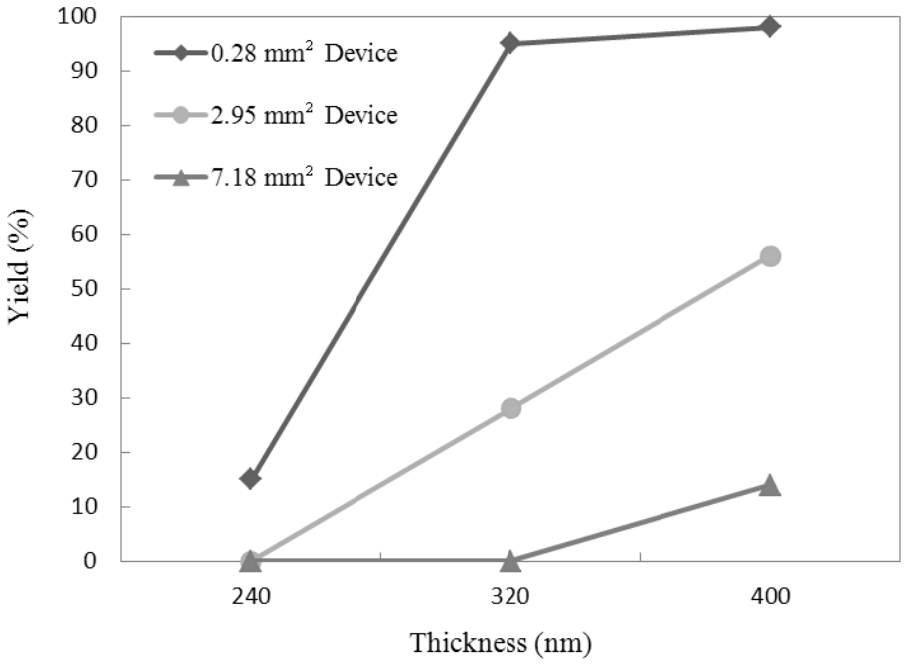


Figure 2.23 Effect of film thickness on PZT device yield

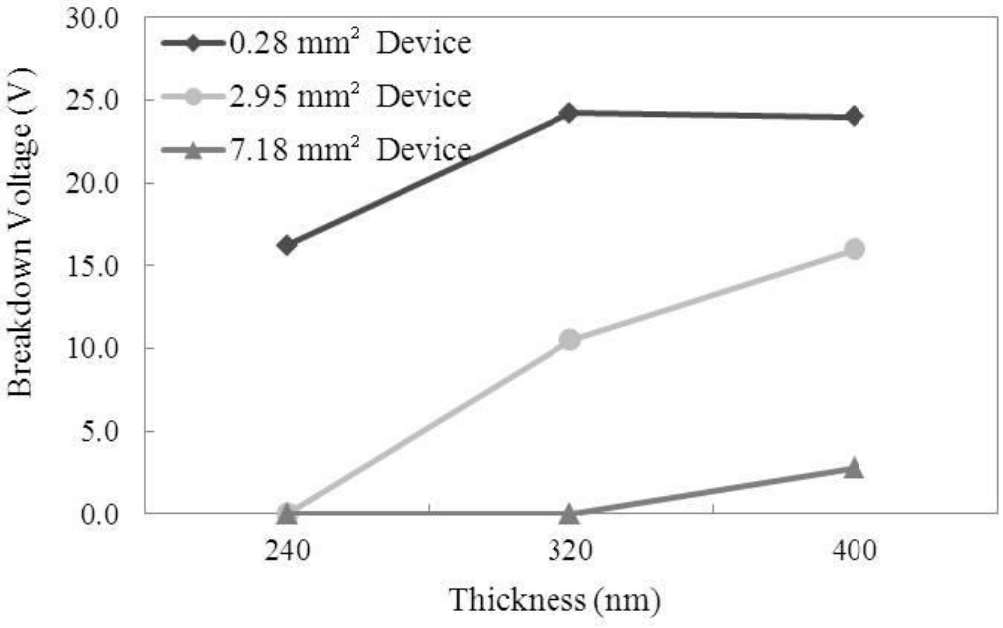


Figure 2.24 Effect of film thickness on PZT breakdown voltage

From the analysis above, it seems plausible to reduce the film thickness in order to improve the capacitance. This would be the case when the dielectric material has absolutely no defects. In reality, however, the thin films under investigation are rarely defect-free, as in the case of almost any sol-gel synthesized thin films. And device failure and breakdown is directly related to defect density in the films, since the defects provide conducting paths that are of less resistance than the surrounding film. As a result, the film is thinned down, the device yield and breakdown voltage both decrease sharply as shown in figure 2.23 and 2.24. The reason is that each coating in the sol-gel process covers the defects formed in the underlying layers, obstructing conducting paths and healing surface pinholes. Obviously, the yield also decreases dramatically with increasing device area since chance of defect inclusion is greater. Theoretically, if the yield for a device with area A is y (y<1), then, assuming the defect density is constant over the whole film, the yield for a device with area nA would be y^n.

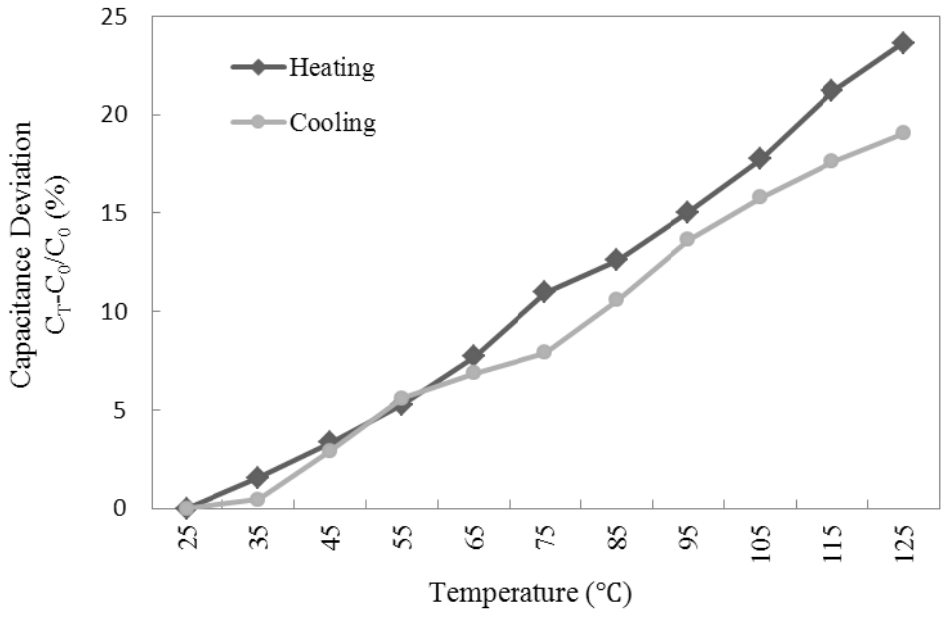


Figure 2.25 Effect of temperature on 400nm PZT device capacitance measured at 100kHz, 1V

(2) Effect of Temperature on Capacitance

The influence of temperature on the capacitance of a typical 400 nm thick, 0.28 mm^2 device is shown in figure 2.25. The capacitance gradually increases with increasing temperature, since the permittivity of PZT increases with temperature below the Curie temperature [1]. The percentage variation of the capacitance value does not exceed 25% when the temperature is cycled from 25 ℃ to 125 ℃, which demonstrates the thermal stability of the device.

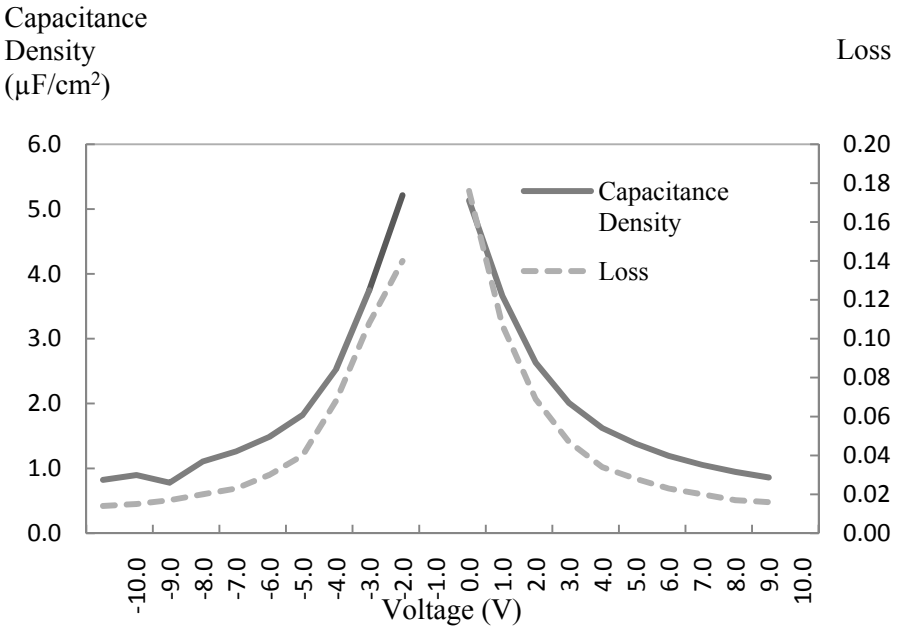


Figure 2.26 Capacitance density of PZT at 100kHz as a function of applied bias

(3) Effect of Applied Bias on Capacitance

The capacitance and loss tangent of a typical 400nm thick, 0.28mm^2 device were measured with different voltage bias at 100 kHz and the result is shown in figure 2.26. The capacitance curve shows almost symmetric behavior at positive and negative biases, and peaked at around ±1V, which corresponds to the coercive field for dipole switching

[34]. The loss curve, however, is not symmetric and may be related to the non-symmetric PZT-Au and PZT-Pt interface.

(4) Leakage Current

Figure 2.27 shows leakage current density as a function of applied bias field for a 400 nm thick, 0.28 mm^2 device.

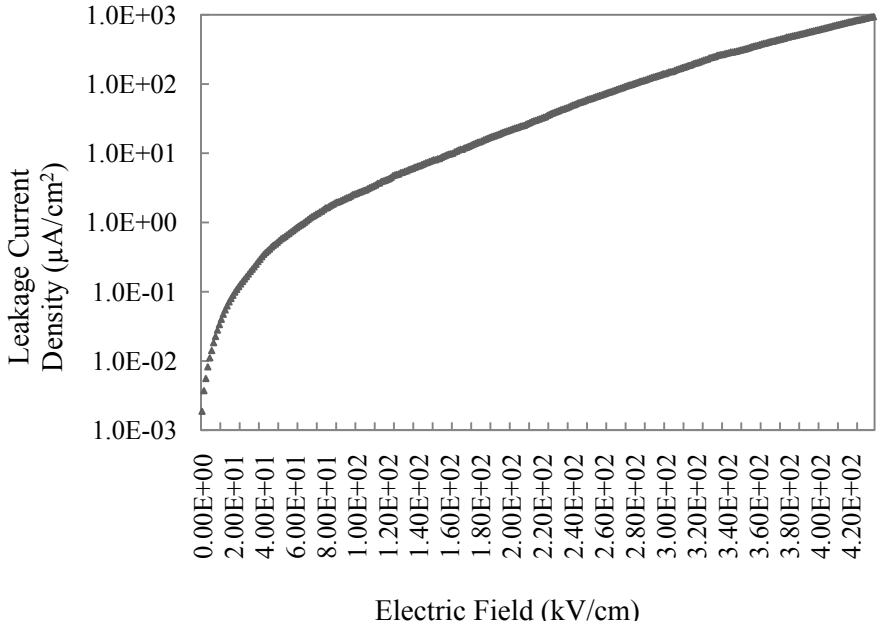


Figure 2.27 Leakage of PZT thin film device under DC condition

2.3.3 Properties of PLZT Thin Films Fabricated on Metal Substrates

2.3.3.1 Effect of PZT Capping and Buffer Layers on Phase Purity

Four types of PLZT thin films were tested on Pt electrodes. They are denoted as:

PLZT(5): 400 nm PLZT

PLZT(4)/PZT(1): 320 nm PLZT with 80 nm PZT capping layer

PZT(1)/PLZT(4): 320 nm PLZT with 80 nm PZT buffer layer

PZT(1)/PLZT(3)/PZT(1): 240nm PLZT, with PZT capping and buffer layer of 80 nm each

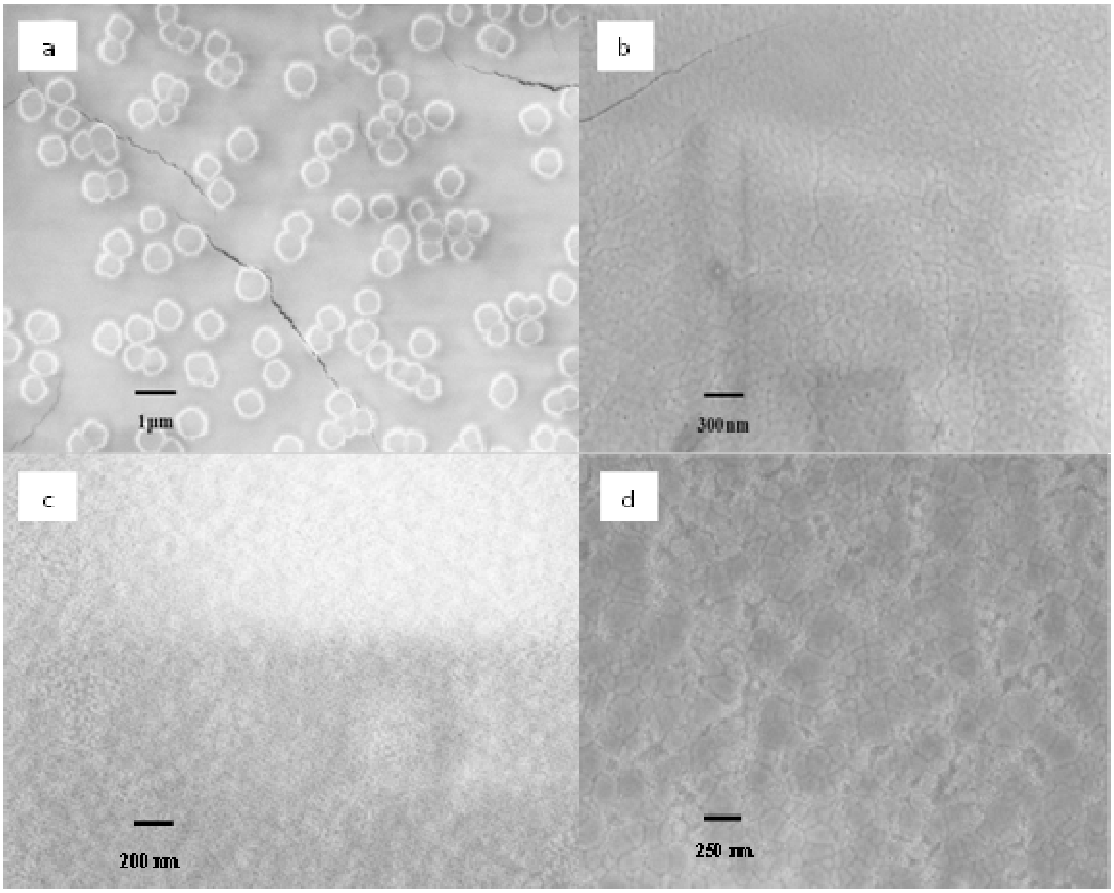


Figure 2.28 Surface morphologies for (a) PLZT(5), (b) PLZT(4)/PZT(1), (c) PZT(1)/PLZT(4) and (d) PZT(1)/PLZT(3)/PZT(1) thin films

The SEM images of their surface morphology after sintering are shown in figure 2.28. For PLZT(5) as in figure 2.28(a), PLZT surface is covered with rosette structure with diameter around 500 nm, indicating that it is not phase-pure. For PLZT(4)/PZT(1) as in figure 2.28(b), the PZT capping layer has suppressed the rosette structure, but the film suffers from severe cracking due to the big volume change of the underlying PLZT when it goes through a phase change during the heat treatment. For PZT(1)/PLZT(4) as in

figure 2.28(c), the film surface is covered by very fine grained rosettes. For PZT(1)/PLZT(3)/PZT(1) as in figure 2.28(d), no cracks or rosettes are found, and the film surface is characterized by large but non-uniform grains.

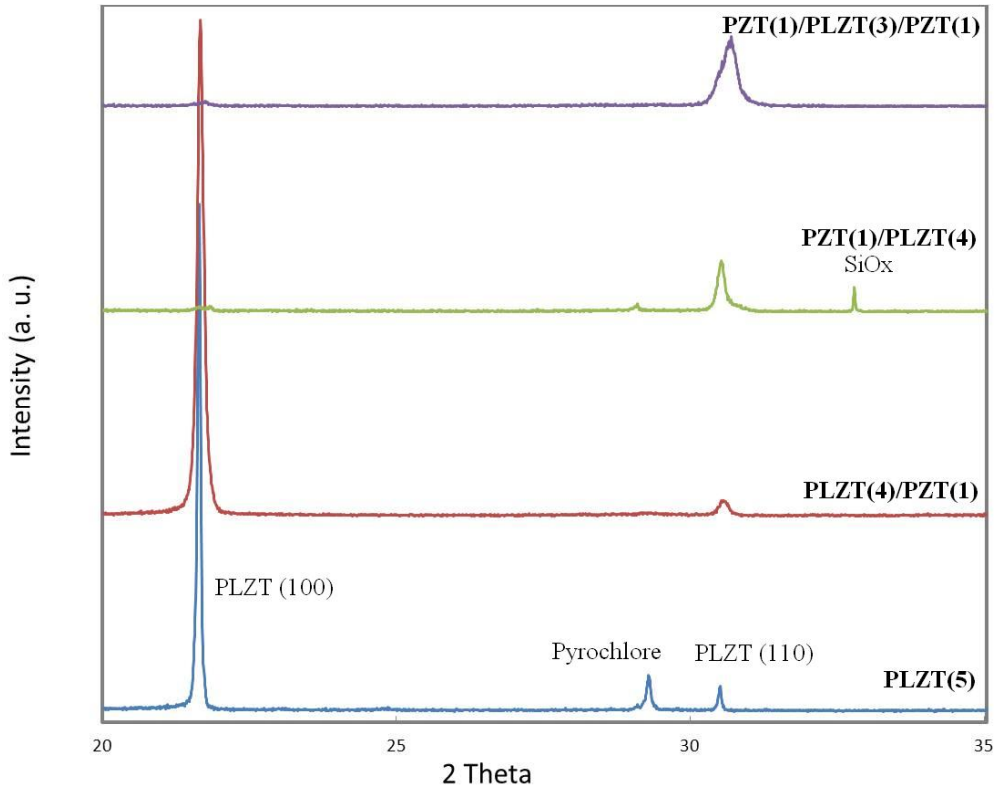


Figure 2.29 XRD of PZT/PLZT samples sintered under identical conditions

XRD on these samples is shown in figure 2.29. Comparing the XRD peaks of the four samples, two observations can be made:

(1) Samples that are without the PZT buffer layer, PLZT(5) and PLZT(4)/PZT(1), showed highly <100> orientation; while samples with the buffer layer, PZT(1)/PLZT(4) and PZT(1)/PLZT(3)/PZT(1), showed a preferred orientation of <110>.

(2) Samples without the PZT capping layer, PLZT(5) and PZT(1)/PLZT(4) showed some crystallization in the pyrochlore phase, while samples with the PZT capping layer, PLZT(4)/PZT(1) and PZT(1)/PLZT(3)/PZT(1), showed no significant pyrochlore formation.

It is therefore concluded that under the process conditions of this study, a PZT buffer layer as well as a capping layer are beneficial for the film crystallization properties.

2.3.3.2 Electrical Characterization of PZT/PLZT/PZT Capacitors

The PZT(1)/PLZT(3)/PZT(1) thin film with thickness of 400 nm and device area of 0.28 mm^2 has been characterized. Measurements were done on 50 devices and average values were taken. The results are summarized in table 2.3. The standard deviation for the measured values is generally less than 10%.

Table 2.3 Electrical Properties and Yield of 400nm PZT/PLZT/PZT Thin Film Capacitors with 0.28mm^2 area on Pt at 100kHz, 1V

Device Area (mm^2)	Capacitance @ 1V (nF)	Capacitance Density @ 1V ($\mu F/cm^2$)	Loss	BDV (V)	Leakage @ 3V ($\mu A/cm^2$)	Yield
0.28	9.85	3.51	0.065	49.2	0.17	92%

Compared to PZT, the PZT/PLZT hybrid devices showed slightly lower capacitance density at 1V. However, the breakdown voltage for these devices is doubled. Higher breakdown voltage not only offers better reliability for capacitor applications, but enables higher operation voltage and higher polling voltage for piezoelectric MEMS applications as well.

It has been found out that the leakage and breakdown in PZT thin films is related to oxygen vacancies present in the crystal [35]. The significant improvement in reliability of the La doped films can be attributed to the effect of donor doping that reduces the p-type oxygen vacancy conduction in PZT thin films [36]. The related defect reactions are:

$$nil \leftrightarrow V_O^{\cdot\cdot} + V_{Pb}''$$

$$nil \leftrightarrow e' + h^{\cdot}$$

$$O_O^{\times} \leftrightarrow \frac{1}{2}O_2 + V_O^{\cdot\cdot} + 2e'$$

$$La_2O_3 \leftrightarrow 2La_{Pb}^{\cdot} + 3O_O^{\times} + V_{Pb}''$$

According to the charge neutrality rule, the defect concentrations in the crystal should satisfy

$$[e'] + 2[V_{Pb}''] = [h^{\cdot}] + 2[V_O^{\cdot\cdot}] + [La_{Pb}^{\cdot}]$$

Therefore, the addition of La suppresses the oxygen vacancy generation, which may lead to the high breakdown field in the PLZT films in this study.

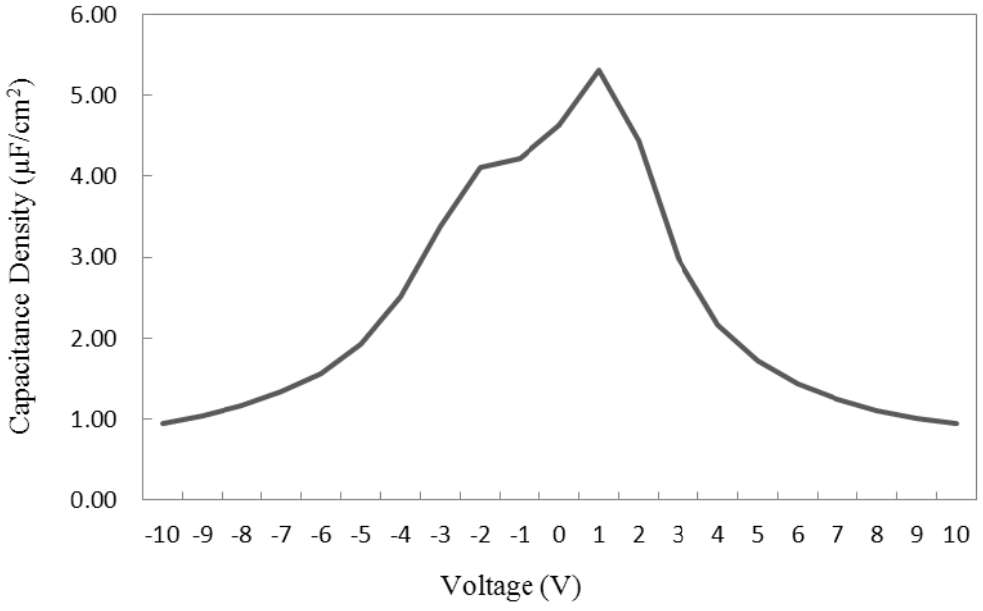


Figure 2.30 Capacitance density of 400nm PZT/PLZT/PZT thin film as a function of applied bias at 100kHz

Capacitance density of the 400 nm PZT/PLZT/PZT thin film was measured as a function of applied bias, and the result is shown in figure 2.30. Different from the result on pure PZT, the PLZT inclusion leads to a shift in capacitance density peak to ±2V.

2.3.4 Properties of PZT Thin Films Fabricated on $LaNiO_3$ Substrates

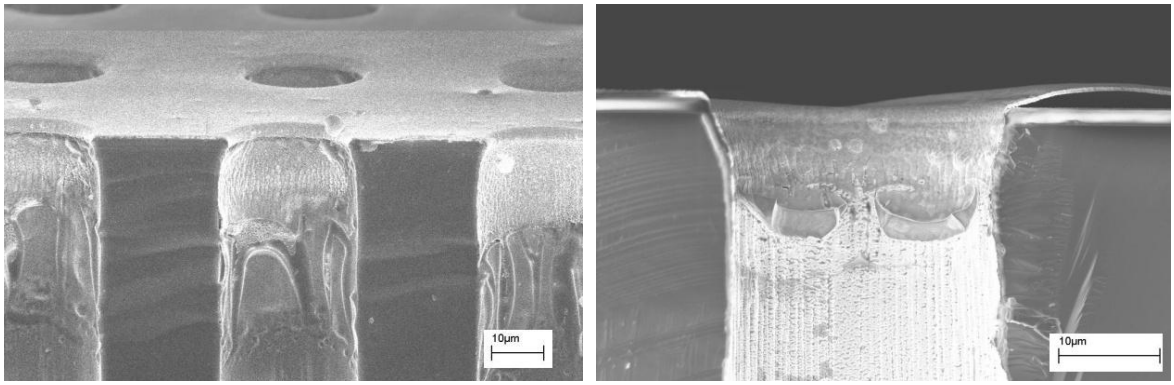
The electrical properties of PZT thin film of 400 nm thick fabricated on $LaNiO_3$ electrode is summarized in table 2.4; only 2.95 mm^2 devices were tested. Measurements were done on 30 devices and average values were taken. The standard deviation for the measured values is generally less than 10%. The devices showed reasonable capacitance values, proving the compatibility of PZT with $LaNiO_3$ under the processing conditions in this study, though slight interdiffusion between the two materials cannot be excluded. Yield for this type of electrode is not as high as on Pt, probably due to the increased surface roughness of the electrode material giving concentrated electric field strength at near the sharp surface morphologies. The capacitance density is slightly lower than that of PZT on Pt electrodes, and loss slightly higher, due to lower conductivity of the electrode and possible interdiffusion.

Table 2.4 Electrical Properties and Yield of 400nm PZT Thin Film Capacitors with 2.95 mm^2 area on $LaNiO_3$ at 100kHz, 1V

Device Area (mm^2)	Capacitance @ 1V (nF)	Capacitance Density @ 1V ($\mu F/cm^2$)	Loss	Yield
2.95	81.01	2.75	0.651	22%

2.3.5 Conformality of Sol-gel Coating on 3-D surfaces

2.3.5.1 Vacuum Assisted Infiltration on Trench Type I

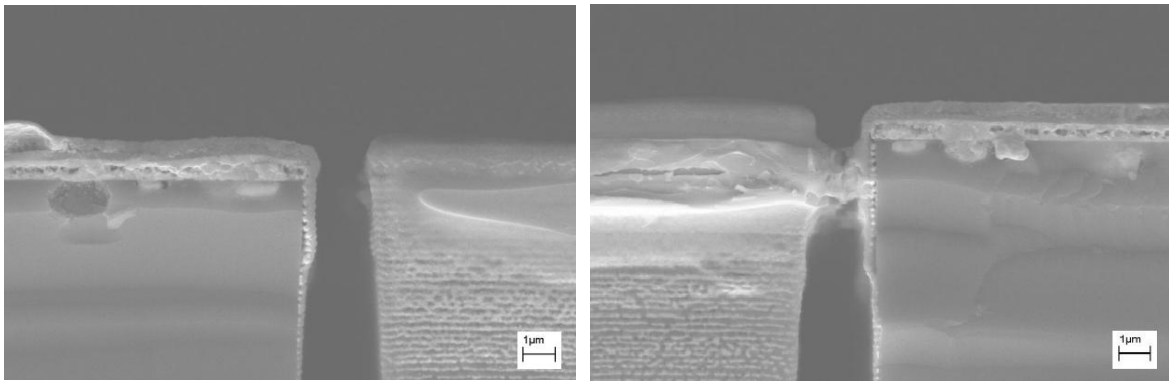


(a) (b)

Figure 2.31 Vacuum infiltration on trench type I: (a) zoom-out view (b) close-up view on a single trench with film peeling

Figure 2.31 shows the cross-sectional SEM image of type I trench after vacuum infiltration and sintering. The air flow through the trench produced a smooth surface on the Si wafer top surface, but the flow of sol inside the trench opening was turbulent, resulting in highly non-uniform coating on the sidewall. In figure 2.31 (b), the film inside the trench peeled off due to extreme non-uniformity in thickness.

2.3.5.2 Direct Spin Coating on Trench Type II



(a) (b)

Figure 2.32 Direct spin coating on trench type I: (a) an unclogged trench (b) a clogged trench

Figure 2.32 shows the cross-sectional SEM image of type II trench after spin coating and sintering. On some of the devices, the sol did cover the trench sidewalls without peeling off, though conformality remains a problem with a thickness variation of ±200% on different positions as indicated in figure 2.32(a). While on other devices, the sol clogged the trench as shown in figure 2.32(b). It was observed that due to the specific mask design, while all trenches were of the same direction on the Si wafer, their relative orientation with respect to the rotation center of the spinner was different: those with trench directions parallel to the radial direction of the spinner got more conformal coatings, and those with trench directions non-parallel to the radial direction were more likely to be clogged.

2.3.5.3 Radial Direction Spin Coating on Trench Type II

From section 2.3.5.2 it is concluded that trench orientation plays an important role in the spin-coating results. The full Si wafers were therefore diced into individual patterned squares with a set of trenches, which were subsequently fixed with the trenches parallel to the radial direction of the spinner. Figure 2.33 shows the cross-sectional SEM images of the resulting coating of $LaNiO_3$ thin film after sintering. Despite the surface roughness of the silicon intrinsic to the ionic etching process, the $LaNiO_3$ was conformally coated on the trenches with full coverage. EDS has confirmed that the $LaNiO_3$ thin film was coated continuously and homogeneously on different positions of the trench as shown in figure 2.34. Thickness of the film is around 150 nm.

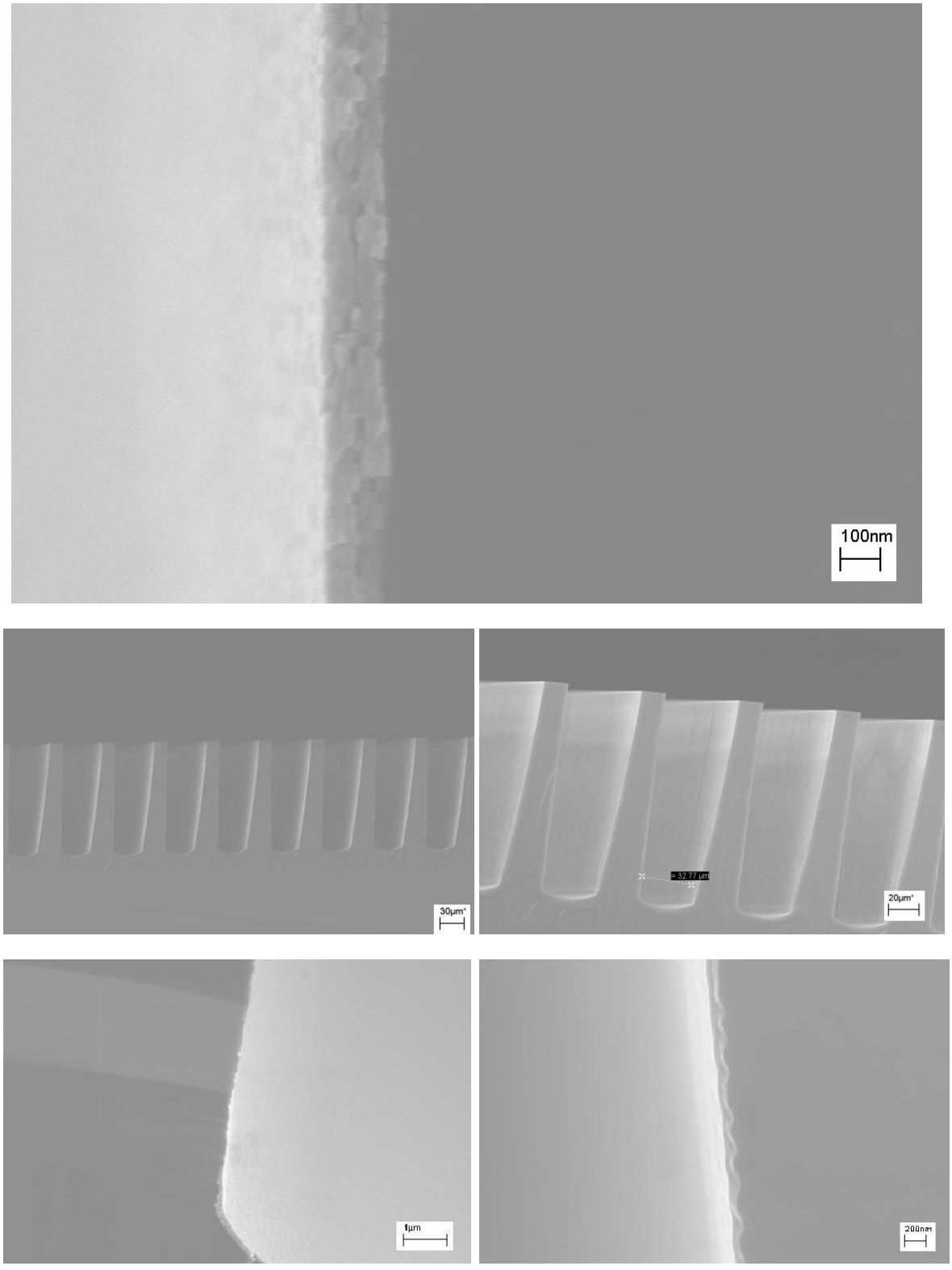


Figure 2.33 Radial direction spin coating on trench type III at different magnifications

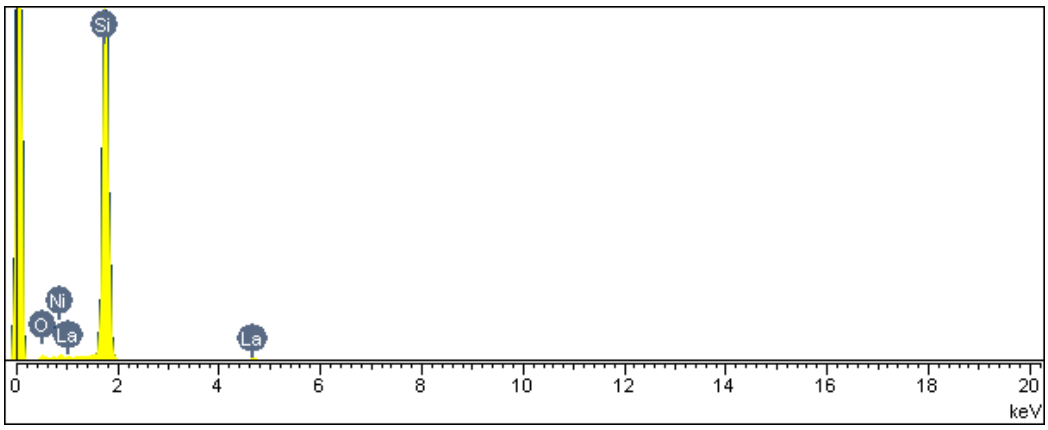


Figure 2.34 Typical EDS spectra of $LaNiO_3$ coating on trenches

2.4 Conclusions and Future Work

$LaNiO_3$ electrodes have been synthesized and deposited on Si wafers with sol-gel method. The critical thickness above which cracking will occur is inferred to be around 200 nm. Highly conducting films have been prepared and though a longer furnace sintering treatment produces larger grain size and higher degree of crystallinity, the conductivity of the films treated by the two sintering methods are comparable.

High quality PZT and PLZT thin films have been synthesized by sol-gel method and deposited on Pt and $LaNiO_3$ electrodes.

With PZT, a high capacitance density of $4\mu F/cm^2$ was achieved on 400 nm films with high breakdown voltage and a high yield of 98% on 0.28 mm^2 devices. 14% yield has been achieved with 7.18 mm^2 devices. The effect of temperature and applied bias on capacitance density has also been characterized.

With PLZT, a new approach using PZT capping layer to ensure phase purity of the film was employed. The PZT capping layer is ferroelectric itself, thus it gives better

performance than the approach proposed by Tania *et al.* [25] in which a non-ferroelectric PbO capping layer was used. A PZT buffer layer is also found to alter the crystal orientation of the PLZT and be beneficial for its electrical performance. Also, addition of PLZT was found to double the breakdown voltage compared to pure PZT without sacrificing the capacitance density. The mechanism of such a reliability improvement can be attributed to the reduction of oxygen vacancy concentration after La addition. Employing the PZT/PLZT/PZT sandwiched structure, the breakdown voltage of the 400 nm thick film was increased to twice of that of the PZT films of the same thickness without sacrificing much of the capacitance density. A capacitance density of 3.5μF/cm^2 was achieved with breakdown voltage of 49V and yield of 92% on 0.28 mm^2 devices.

Compatibility of PZT with $LaNiO_3$ electrode has been demonstrated. Although the device performance is not as good as on Pt electrodes, further optimization of the process can potentially achieve the final goal of 3-D integration.

Finally, low-cost, conformal thin film coating on 3-D surfaces was demonstrated with Si trenches with their orientation parallel to the spinner radial direction for the first time. Step coverage of 100% was demonstrated with reasonably conformal coating thickness. This demonstrates that the sol-gel technology on planar devices is extensible to 3-D surfaces and opens up potential device possibilities for both capacitor and MEMS applications.

Recommended future work includes:

(1) Optimization of $LaNiO_3$ process to achieve better property of PZT/$LaNiO_3$ combination. Effect of $LaNiO_3$ crystal orientation on PZT texture should be characterized, and it is recommended that a barrier oxide layer, such as ZrO_2 is added between $LaNiO_3$ and Si to minimize diffusion.

(2) Optimization of the sol-gel process so that higher yield on large area devices can be achieved. One reason for defect formation in sol-gel process is that the precursors are highly moisture-sensitive and some precipitates forms unavoidably during handling, even within Ar environment. Two approaches can be employed in an effort to reduce precipitation:

A. Filtering the sol before spin-coating so that precipitates above a certain size are eliminated from the sol.

B. Using extremely dilute sol concentrations and increasing the number of coatings, which gives greater chance of defect healing and coverage.

C. Employ chelating agents to suppress the moisture-sensitivity of the chemicals, which requires extensive research and optimization.

Once yield on a large area device is improved, 3-D devices can be demonstrated using the conformal coating technique described in section 2.3.5.3.

(3) Exploring the limitations of the radial spin-coating technique. As the trench size shrinks down, the radial spin-coating is expected to meet some difficulties due to turbulence formation in very thin channels. It is therefore highly desirable to explore the limitations of this method and evaluate its applicability to smaller feature sizes.

CHAPTER 3

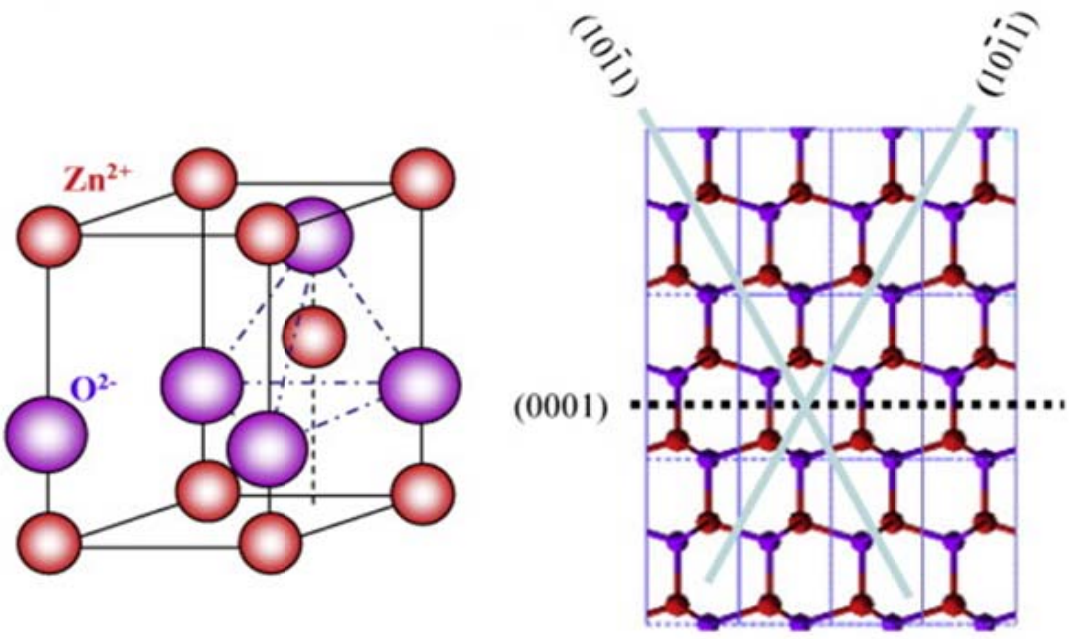
SYNTHESIS AND CHARACTERIZATION OF PIEZOELECTRIC ZINC OXIDE AND GALLIUM NITRIDE NANOWIRES

3.1 Background

3.1.1 Crystal Structure and Properties

3.1.1.1 Crystal Structure

The thermodynamically stable structure at room temperature for ZnO and GaN is the Wurtzite structure, which belongs to the hexagonal space group $P6_3mc$. A schematic representation of the ZnO structure is shown in figure 3.1 [37].



(a) (b)

Figure 3.1 Crystal structure of ZnO: (a) lattice structure and (b) atomic layers viewed from normal to c-axis [17]

The Wurtzite structure of ZnO can be seen as hexagonal close packed O^{2-} with 50% of the tetrahedral sites filled by the Zn^{2+}. The lattice constant *a* for ZnO is 3.26 Å, with an c/a ratio of 1.616 [38]. The coordinate numbers for the zinc and oxygen ions are both four. The [0001] direction, or the c axis direction, is defined as the direction in which Zn^{2+} points to O^{2-}, and vice versa for the $[000\bar{1}]$ direction. As is obvious from figure 3.1 (b), the structure consists of alternating Zn atom layers and O atom layers. The (0001) face is Zn terminated, and the $(000\bar{1})$ face is O terminated; therefore, the properties of (0001) and $(000\bar{1})$ surfaces are different, leading to polar surfaces in ZnO. Bonding in zinc oxide has a great ionic extent, and therefore ZnO nanocrystals can dissolve in water if exposed to water for long enough.

The structure for GaN is the same as ZnO, with Ga and N tetrahedrons stacking in an interpenetrating manner throughout the whole structure. The lattice constant *a* for GaN is 3.198 Å, with a c/a ratio of 1.634 [39]. The crystallographic directions and faces are similarly defined. As III-V compound, the bonds in GaN tend to have less ionic nature in them, and therefore GaN is insoluble in water and more chemically stable.

3.1.1.2 Piezoelectric Properties

The lack of centrosymmetry of the Wurtzite structure gives rise to the piezoelectricity of ZnO and GaN. When stress is applied on a ZnO or GaN crystal, the center of mass of anions and cations no longer overlap. This process induces a net dipole moment, producing piezoelectric charge across the material. These charges result in a built-in electric potential, or the piezopotential. This is the piezoelectric effect of ZnO and GaN.

Conversely, when an electric field is applied on a ZnO or GaN crystal, the ions also shift positions, yielding strain in the material which manifests the converse piezoelectric effect. Theoretical calculations have shown that with applied electric field E in the c axis

direction, the Zn1-O1 bond is compressed and Zn2-O1 bond is rotated such that the crystal dimension shrinks in the c axis direction, as shown in figure 3.2 [40].

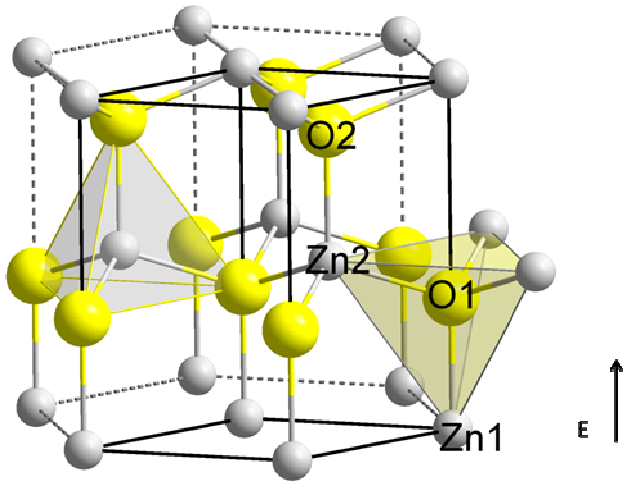


Figure 3.2 Microscopic origin of the converse piezoelectric effect in ZnO [40]

Table 3.1 Piezoelectric coefficient for ZnO and GaN in different material forms

Material	d_{33} (pC/N)
ZnO (single crystal)	12.4 [41]
ZnO (c-axis oriented thin film)	2.0-13.0 [41]
ZnO (nanobelt)	14.3-26.7 [42]
GaN (single crystal bulk)	3.7 [43]
GaN (single crystal thin film)	2.8 [43]
GaN (c-axis oriented thin film)	2.7 [44]

The piezoelectric coefficient for ZnO and GaN in bulk, thin film and nanobelt forms are listed in table 3.1. ZnO nanostructures have a piezoelectric coefficient two to three times of that of the bulk form. Moreover, unlike bulk crystals which typically crack under

strains that are greater than 2%, nanowires can stand higher strains without fracture, and since nanowires are normally dislocation free, they don't fatigue like bulk materials. These excellent properties make ZnO and GaN promising materials for piezoelectric applications.

Traditional piezoelectric materials, such as PZT and PMN, are insulators, and therefore the piezopotential only produces an effect on the surface of the crystal or in the external circuit, and will not affect the internal conduction properties. However, when semiconductors such as ZnO and GaN are used, the piezopotential in the crystal can affect the behavior of the carriers in ZnO and GaN. For nanowire systems, the contact resistance is typically 2-10 times the resistance of the nanowire [45]. Therefore, combined with proper electrical contacts, the conduction properties can be tuned by strain in the crystal. This is the basis for piezoelectronics [46].

3.1.1.3 Semiconducting Properties

ZnO is a wide bandgap semiconductor with bandgap 3.37eV and a high exciton binding energy (60 meV) at room temperature [47]. GaN has a bandgap of 3.51 eV with an exciton binding energy of 28 meV [43]. They are both direct bandgap materials suitable for optic and optoelectronic applications.

The conductivity is highly affected by the point defects formed during the synthesis. For ZnO, the most common point defects are oxygen vacancies:

$$O_O^{\times} \rightarrow \frac{1}{2}O_2 + V_O^{\cdot\cdot} + 2e'$$

Typically, the synthesis process will unavoidably introduce a great amount of oxygen vacancies. ZnO is therefore natively n-type. The defect levels for all possible point

defects in GaN in the bandgap are illustrated in figure 3.3 [48]. The number in the figure denotes the charge of the defect.

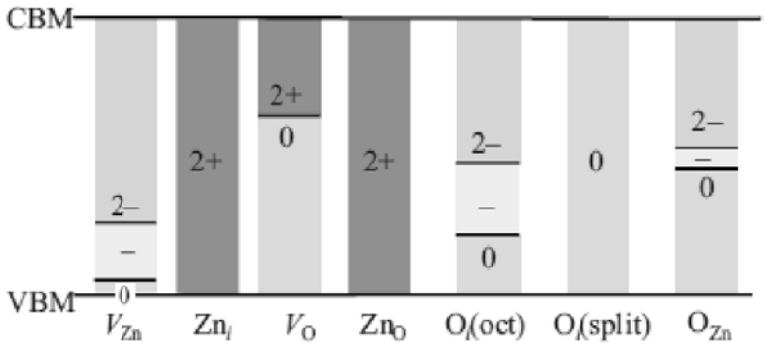


Figure 3.3 Point defects in ZnO [48]

For ZnO single crystals, the mobility at room temperature is around 180 cm^2/Vs [49]. The value for thin films and nanowires is lower, limited by defect, impurity and surface scattering [50]. For thin films, a mobility of 115-155 cm^2/Vs is reported [51], while the typical values for nanowires range from 6.4 cm^2/Vs to 30cm^2/Vs. However, surface passivation for the nanowires can lead to mobility as high as 3118 cm^2/Vs [52].

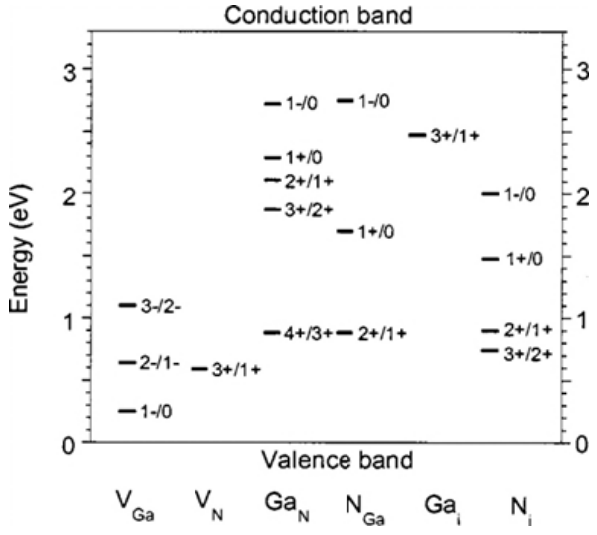


Figure 3.4 Point defects in GaN [53]

For GaN crystals, the most common defects introduced by the growth process are gallium vacancies and therefore they are natively n-type, too. The defect levels for all possible point defects in GaN in the bandgap are illustrated in figure 3.4 [53].

The electron mobility for GaN thin film generally falls into the range of 60-100 cm^2/Vs [54]. For nanowires, the mobility depend highly on the synthesis process, and the value is typically 2-10 cm^2/Vs [55] while values as high as 600 cm^2/Vs have been reported [56].

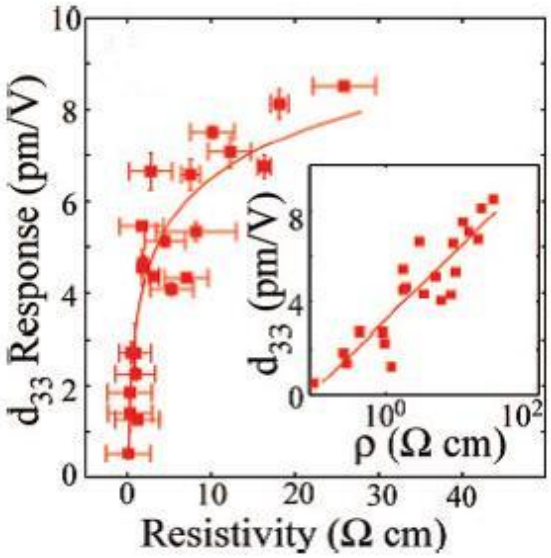


Figure 3.5 Piezoelectric coefficient as a function of resistivity for ZnO [50]

It is noteworthy that the semiconducting properties and piezoelectric properties are not independent. In fact, the conductivity of the crystal has great influence on the piezoelectric properties. Figure 3.5 shows the measured piezoelectric coefficient of ZnO nanorods as a function of resistivity [50]. The piezoelectric coefficient is greatly reduced with increasing carrier concentrations. This is explained by the free electron screening of the Madelung constant, thus reduction of the ionic bond strength. The relationship

between piezoelectric coefficient and resistivity for GaN has not been reported. However, it is speculated that the piezoelectric coefficient for GaN should be less sensitive to its conductivity, due to less ionic component in the Ga-N bonds.

3.1.1.4 Metal-semiconductor Contact

The semiconducting properties of ZnO and GaN lead to two possible types of contacts when they are connected with a metal: Ohmic contact and Schottky contact. An Ohmic contact is defined as one with a negligible contact resistance, while a Schottky contact forms a barrier that theoretically equals to $q(\varphi_m-\chi)$ for n-type semiconductors, where q is the electronic charge, $q\varphi_m$ is the work function of the metal, and $q\chi$ is the electron affinity of the semiconductor [57]. In reality, the Schottky barrier height is highly dependent on the interface. Schottky barrier height can be tuned by strain induced piezopotential, which is the basis for piezotronics [46].

3.1.2 Synthesis Method

3.1.2.1 Physical Vapor Deposition

(1) Vapor-liquid-solid and Vapor-solid Growth Mechanism

In Vapor-liquid-solid (VLS) growth mechanism, a foreign catalyst (usually metal) is used [58]. Normally, a thin metal film a few to a few tens of nanometers thick is deposited onto the substrate. During the initial stage of growth, as the temperature in the reaction chamber rises, the catalyst film is first broken into molten droplets covering the substrate area, which is shown in figure 3.6 (a). Subsequently, the source vapor is incorporated into the droplets by direct adsorption onto the liquid or by adatom diffusion along the substrate until they meet one of the droplets as shown in figure 3.6 (b). As the content of the source material is increased, supersaturation in the droplet is reached and the material precipitates out, gradually forming a wire with the same diameter as the droplet. At this stage, subsequent source vapor incorporation requires the adatoms to diffuse not only on

the substrate surface, but also on the nanowire surface before they get to the catalyst droplet. Finally, as the growth process stops, the nanowire ends up with a solidified metal cap on top, as illustrated in figure 3.6 (c).

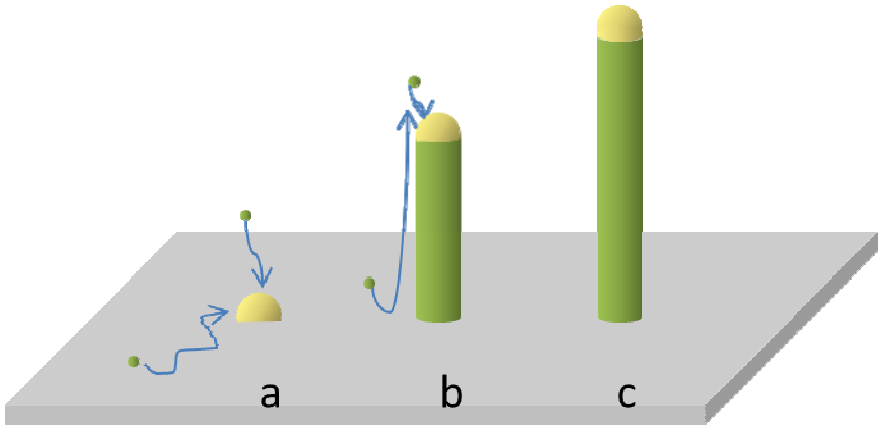


Figure 3.6 VLS growth mechanism: (a) catalyst melting (b) nanowire growth (c) final nanowire

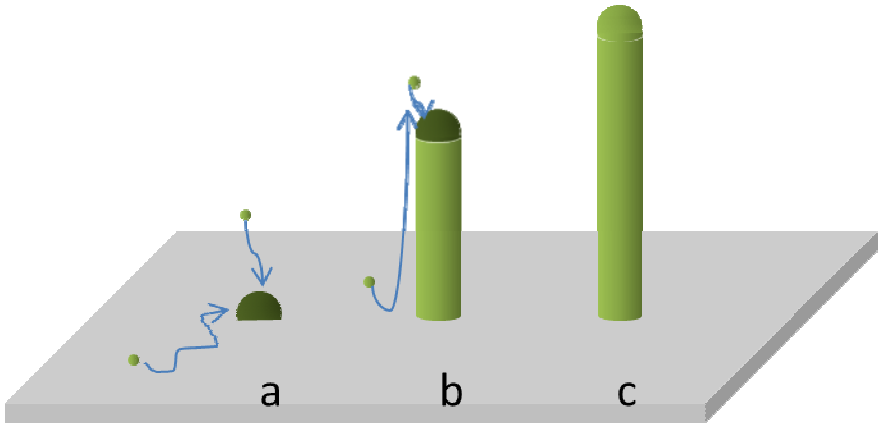


Figure 3.7 VS growth mechanism: (a) non-foreign catalyst melting (b) nanowire growth (c) final nanowire

In VS growth, the mechanism is similar, but the catalyst is not in its liquid form. For example, the catalyst particle for ZnO growth can be oxygen-rich Zn droplets or semi-

molten ZnO droplets [58]. As the catalyst is of the same element as the nanowire material, the metal catalyst particle is not observable on the final nanowire in this case, as is shown in figure 3.7.

Many process parameters such as pressure, temperature and the rate at which temperature is raised all affect the nanowire growth greatly. The adatom diffusion along the substrate as well as nanowire surface is driven by the chemical potential gradient between its initial position and inside the catalyst. On the other hand, the driving force for precipitation is supersaturation inside the catalyst. Therefore, the right condition to enable continuous nanowire growth should provide the right supersaturation in the catalysts, so that it is high enough to sustain precipitation but low enough to maintain adatom diffusion.

Even with the same set of parameters, the nanowire growth can also be influenced by the substrate and catalyst materials used. During the initial stage of the nanowire growth, nucleation takes place on the surface of the substrate. Therefore, it is highly desirable to minimize the interfacial energy. Using a substrate that is lattice-matched with the nanowire will often help promote nucleation and epitaxial growth.

(2) Deposition Techniques

Tube Furnace

The tube furnace is the most simple and cost-effective equipment for vapor phase deposition. It mainly consists of a programmable controller, a cylindrical cavity surrounded by heating coils which heat up the chamber according to the program, temperature feedback system based on a thermocouple, as well as vacuum and gas supply system. The cylindrical tube is commonly made with quartz or alumina and embedded in a thermally insulating medium. The whole furnace may be divided into several heating zones from which a certain temperature gradient can be derived. Or the temperature

gradient can be introduced by cooling at the tube ends. A schematic drawing of the tube furnace is shown in figure 3.8 [59]. During the nanowire growth, the source material in solid phase and the substrate are put inside the chamber; the tube is first pumped down to the desired pressure, and then heated to the desired reaction temperature up to a maximum of 1800 ℃. Gaseous source and/or inert carrier gas is then fed into the chamber to facilitate growth. Finally, the temperature is lowered after growth stops.

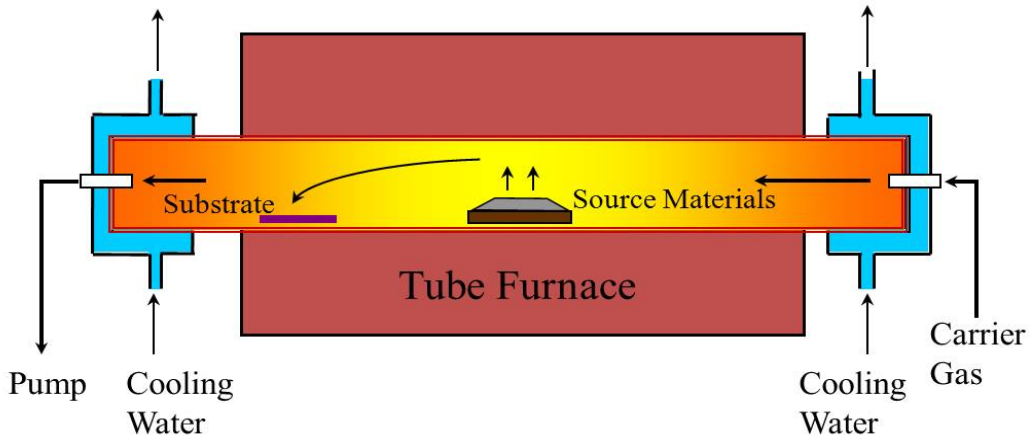


Figure 3.8 Tube furnace set-up for nanowire growth [59]

Metallorganic Chemical Vapor Deposition (MOCVD)

The only difference between the set-up of MOCVD process for nanowire growth and for thin film growth which was introduced in section 2.1.2.2 is that the substrate for nanowire growth is loaded with catalyst to promote one-dimensional growth. Also, conditions such as the growth temperature, source ratio and chamber pressure will be slightly different for nanowires from those for thin films of the same material.

Due to the ability to finely control the source injection, i.e. the source type, ratio and on or off, MOCVD growth offers the ability to grow heterojunctions on the lateral and radial

direction in-situ within the same nanowire. The drawback of the technique is that costly equipment and source are needed, and extensive process optimization is required.

Molecular Beam Epitaxy (MBE)

In molecular beam epitaxy, the chamber is pumped to high vacuum and the elemental source is heated directly to sublimation. The gaseous elements are then sucked into the vacuumed chamber and deposited on the substrate surface where they may react to form the desired product. The resulting growth is extremely slow but films of very high quality and good epitaxial relationship can be obtained. The structure of an MBE chamber is illustrated in figure 3.9 [60].

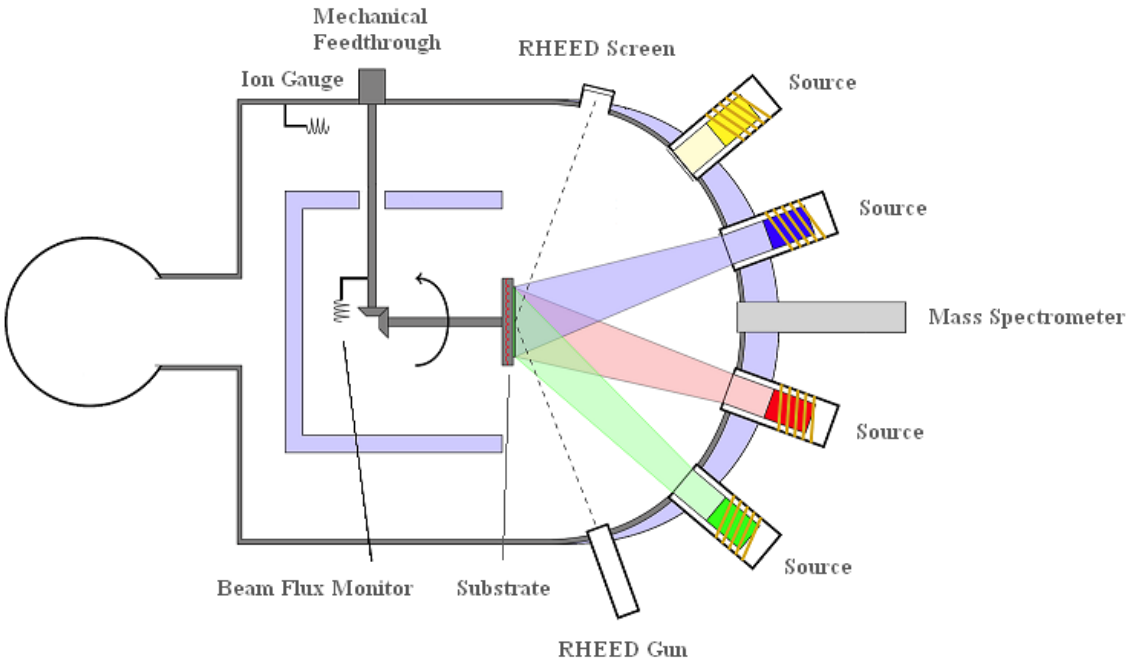


Figure 3.9 Structure of an MBE chamber [60]

MBE offers excellent control over growth down to one atomic layer scale and therefore also offers the ability to grow intricate heterostructures. Nanowires grown by MBE

typically have lower carrier concentrations than those derived from MOCVD [61]. The drawback again is the high equipment and material cost.

Pulsed Laser Deposition (PLD)

The deposition mechanism of PLD is introduced in section 2.1.2.1. The PLD nanowire growth employs much higher pressure (a few Torr) as compared to thin film deposition (usually in the mT range). Also, deposition by PLD sometimes does not require any catalyst, and it is speculated that the molten particulates ejected from the target during deposition serves as the catalyst, resulting in nanowires without metallic caps. The density, aspect ratio and doping can be controlled with this technique [62].

3.1.2.2 Hydrothermal Synthesis

Hydrothermal synthesis of nanowires and nanocrystals employs low temperature and simple process, and is therefore a promising method for nanowire synthesis. The key to induce one-dimensional growth is the utilization of a capping agent which selectively absorbs on the side surfaces of the crystal to inhibit growth [63]. However, the quality of the crystals derived from this process is often inferior to those fabricated by the vapor phase methods, due to possible incorporation of hydroxyl groups and other contaminants. The method is also mostly limited to oxide material synthesis due to the employment of water as the solvent, though some non-oxides can be synthesized by solvothermal methods.

For ZnO nanowire synthesis, the nutrient solution is typically composed of a 1:1 ratio of zinc nitrate and hexamethylenetetramine (HMTA). The substrate is then floated on the solution and heated in an oven over the desired period of time. Five chemical reactions have been proposed to control the growth process [63]:

$$(CH_2)_6 + 6H_2O \leftrightarrow 4NH_3 + 6HCHO$$

$$NH_3 + H_2O \leftrightarrow NH_3 \cdot H_2O$$

$$NH_3 \cdot H_2O \leftrightarrow NH_4^+ + OH^-$$

$$Zn^{2+} + 2OH^- \leftrightarrow Zn(OH)_2$$

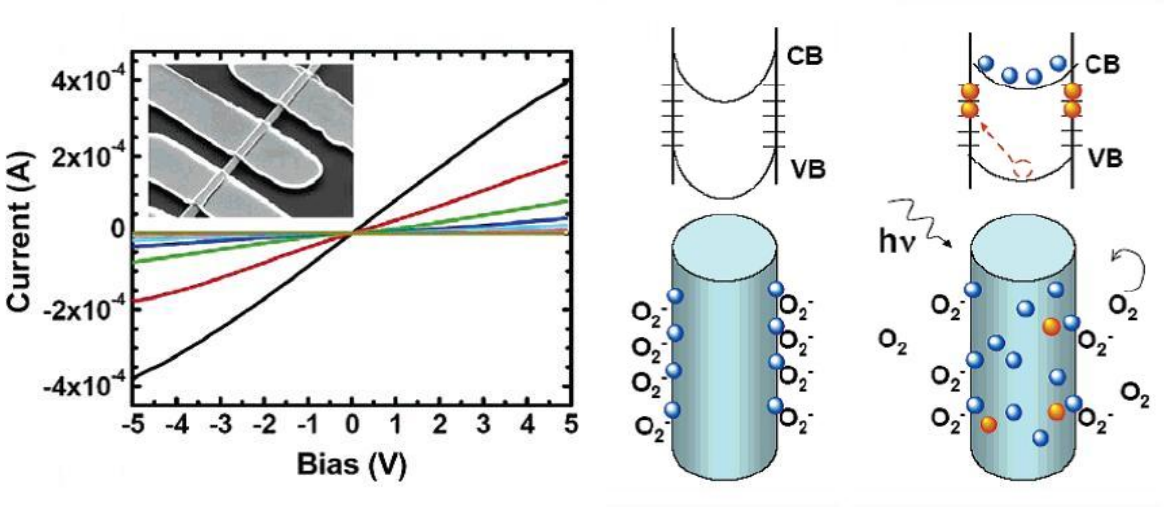
$$Zn(OH)_2 \leftrightarrow ZnO + H_2O$$

And the growth can be controlled by the growth temperature, precursor concentration and growth time.

3.1.3 Applications

3.1.3.1 Optoelectronics

With a direct bandgap, ZnO and GaN nanowires are good candidates for visible-blind UV photodetectors [64] and light-emitting diodes [65]. We hereby emphasize their applications in photo-detection due to the focus of this study.



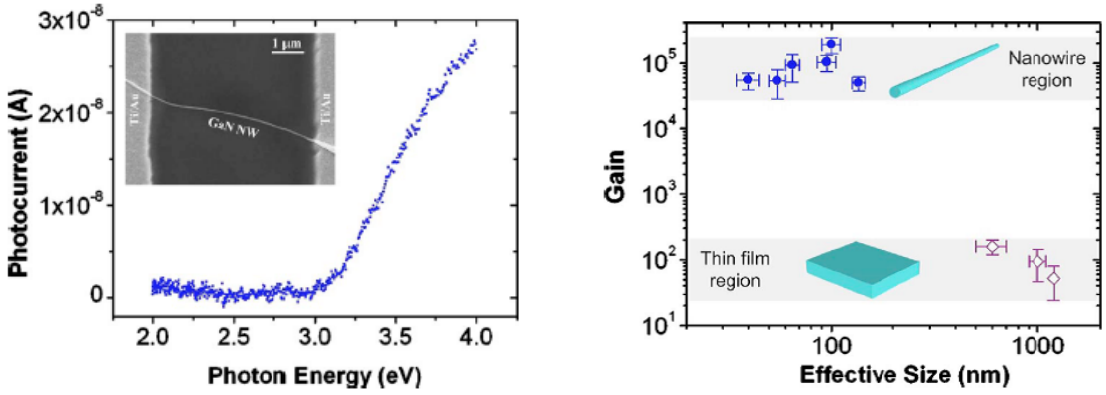
(a) (b) (c)

Figure 3.10 (a) Photoresponse at different illumination intensities and (b), (c) mechanism for ultrahigh gain of ZnO nanowires [64]

Photodetectors with high internal gain have been demonstrated with tube furnace grown

ZnO nanowires and figure 3.10 (a) shows the measured I-V characteristics at various light intensities with wavelength of 390 nm in standard ambient conditions [64]. An internal gain as high as 10^8 was reported. The ultra-high gain was attributed to the oxygen absorption on the nanowire surface and domination of the surface effects due to the high surface-to-volume ratio of nanowires. In dark conditions, the oxygen molecules absorbed capture electrons, resulting in a thin depletion layer near surface in which the bands bend upward as shown in figure 3.10 (b). When illuminated, photogenerated holes are swept to the surface and trapped, which prolongs the lifetime of the unpaired electrons, as shown in figure 3.10 (c).

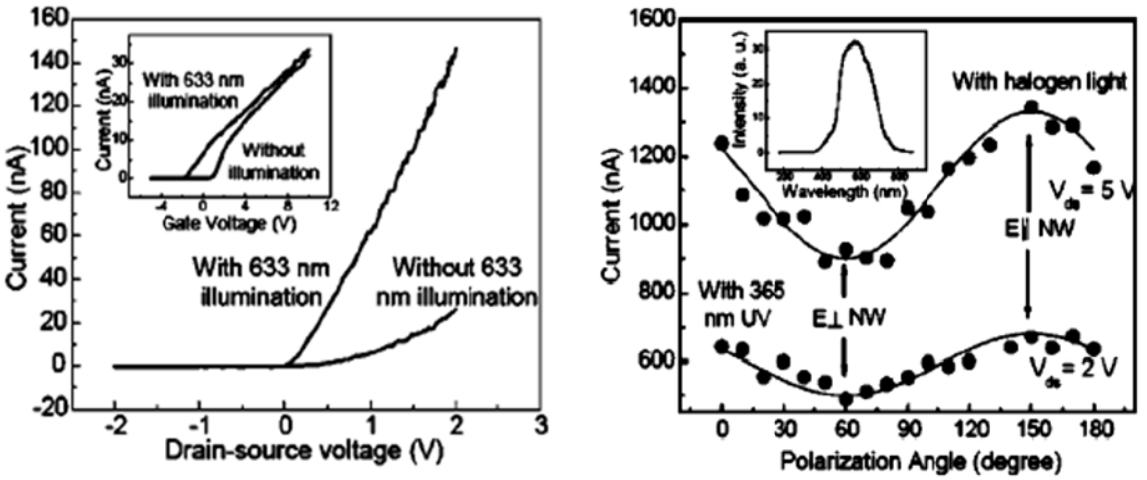
Ultra-high photocurrent gain has also been demonstrated with single GaN nanowires [61]. Gain values up to 1.9×10^5 have been reported. Figure 3.11 (a) is a typical photocurrent spectrum of a 130 nm thick GaN nanowire grown along the m-axis. The photocurrent gain achieved is three orders of magnitude higher than traditional GaN thin film photodetectors as indicated in figure 3.11 (b).



(a) (b)

Figure 3.11 Photocurrent and gain of GaN nanowires [61]

Moreover, the highly anisotropic nature of the nanowire structure can lead to polarization sensitive light detection [10]. Figure 3.12 (a) shows the I-V response of ZnO nanowires with 30-150 μm in diameter under 633 nm laser illumination. The photoresponse to below-bandgap wavelengths in this case is due to defect related deep electronic states. Figure 3.12 (b) shows the photoresponse of the same device as a function of polarization angle for two light sources: 365 nm UV laser and halogen lamp with a center wavelength of around 500 nm. The photocurrent exhibited a clear dependence on polarization. The dependence was attributed to the attenuation of the electric field component of the light normal to the wire axis due to confinement when the nanowire diameter is much smaller than the wavelength [10]. This results in a $\cos^2\theta$ dependence of the photocurrent, where θ is the angle between the polarization of incident light and the nanowire axis.



(a) (b)

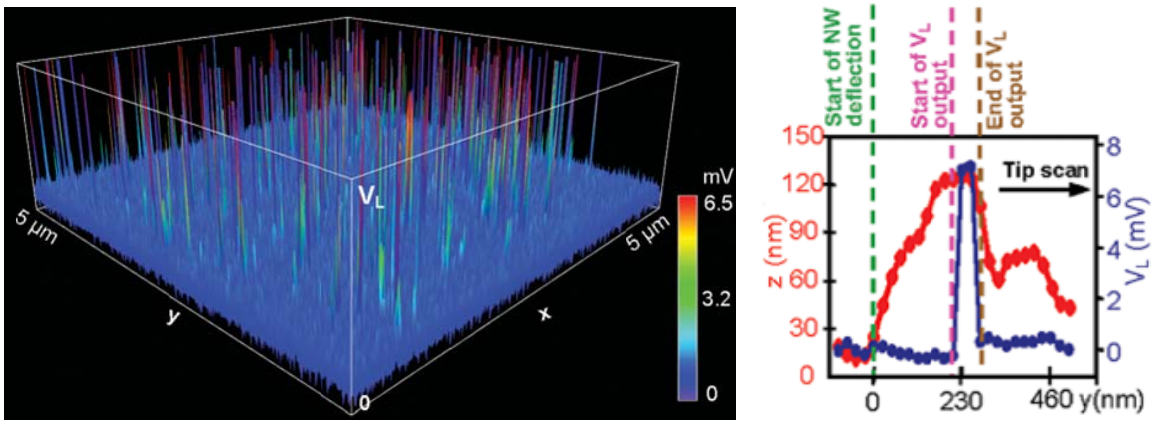
Figure 3.12 (a) photoresponse of ZnO nanowires with 633 nm illumination and (b) polarization sensitivity of the photocurrent [10]

3.1.3.2 Nanogenerators

Energy conversion has been achieved in piezoelectric power generator devices using ZnO and GaN nanowires combined with a Schottky junction to regulate the current flow. The

term “nanogenerator” was first coined in 2006 [66] and since then energy harvesting and conversion have been demonstrated with several device designs based on the same operation principle [67, 68].

In the original design of nanogenerator [66], ZnO nanowire arrays were grown on Al_2O_3 substrate with a ZnO thin film contacting all the nanowires. An AFM tip coated with Pt was used to contact the nanowires while the ZnO thin film was contacted as another electrode, and the voltage signal profile recorded when the tip scanned over the nanowires is shown in figure 3.13 (a). The voltage output was compared to the topography profile acquired from the same scan in figure 3.13 (b) and it was found that the voltage peak corresponds to the tip when touching the compressed side of the nanowire.



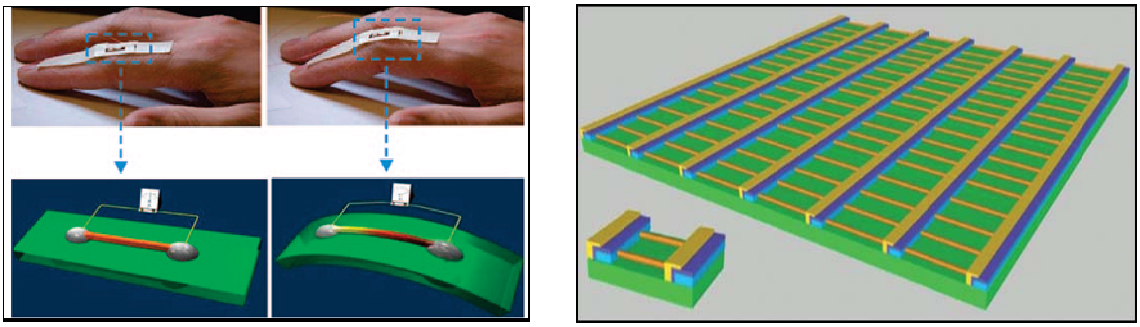
(a) (b)

Figure 3.13 (a) Voltage signal measured on a ZnO nanowire array (b) topography profile of one ZnO nanowire [66]

The voltage output was attributed to the combined effect of piezoelectricity of the nanowires and Schottky contact with the tip. When the nanowire is bent, the piezopotential is positive at the stretched side, and negative at the compressed side. As

the tip touches the stretched side, the Schottky barrier is reversely biased, and current is blocked. When the tip comes into contact with the compressed side, however, the Schottky barrier is forward biased and current flows from the tip to ZnO. The output of ZnO nanogenerator was raised to 0.1-0.15V by a series connection of four single nanowire generators, shown in figure 3.14 (a) [67], and later to 1.26V by large scale lateral integration of 700 rows of ZnO nanowires as shown in figure 3.14 (b) [68]. A self-powered nanowire pH sensor and UV sensor have also been demonstrated, demonstrating a self-sustained system composed entirely of nanowires [68].

A similar device has been demonstrated with GaN nanowire arrays, and piezoelectric output voltages of 0.15-0.35V have been achieved [2].



(a) (b)

Figure 3.14 (a) Single ZnO fine wire generator (SWG) [67] and (b) integration of 700 row of nanowire nanogenerator [68]

3.1.3.3 Piezotronics

The term piezotronics was first coined in 2007 denoting electronics with the piezopotential as the gate voltage [69]. The principle of such a device was demonstrated with ZnO nanowires [70]. The configuration is shown in figure 3.15, in which the ZnO nanowire was deformed by a probe with the other end fixed. At first contact, the nanowire and the tip made an Ohmic contact (figure 3.15 a, b). When the wire was

deflected, the piezopotential in the wire produced a Schottky barrier with the tip, making the I-V characteristic non-symmetrical, and as the defection increased, the barrier height was increased as well (figure 3.15 c-h). Thus the electron transport properties of the device can be tuned by strain. A similar device was later demonstrated with silver paste contacts [11], and by combining several of such devices, logic gates of different functions that are controlled solely by strain can be built [71].

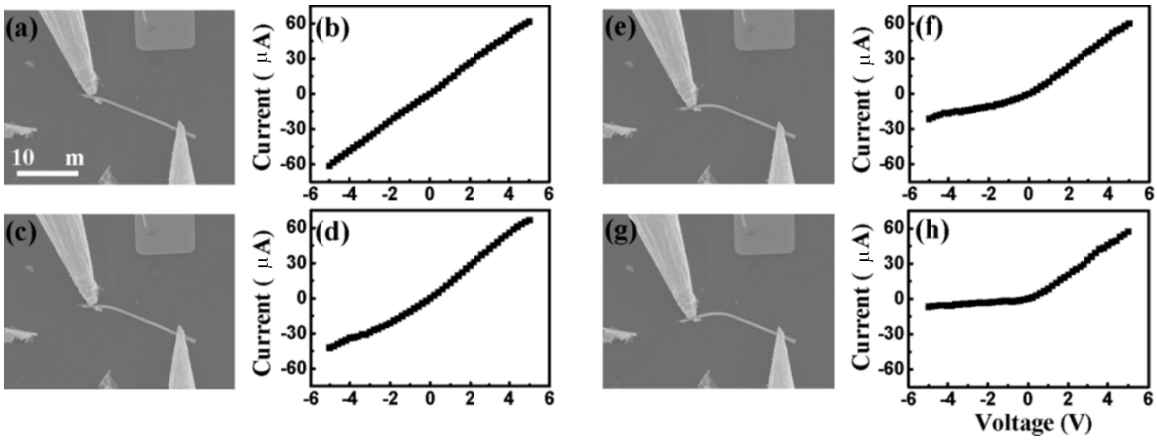


Figure 3.15 Current transport properties of a ZnO nanowire under different straining conditions [70]

3.1.3.4 Piezo-phototronics

Piezo-phototronic effect is defined as the tuning and controlling of electro-optical processes by strain induced piezopotential [46]. As described in section 3.1.3.3, strain induced piezopotential can increase or decrease the Schottky barrier height, while carrier injection by above-bandgap laser illumination can effectively decrease the barrier height; thus the carrier transport properties can be tuned from Schottky to Ohmic or from Ohmic to Schottky by controlling the two factors [72]. Figure 3.16 (a) shows the experimental set-up in which strain and laser can be applied simultaneously on a ZnO microwire. Figure 3.16 (b) shows the tuning of I-V characteristics by applying compressive strain

only, and figures 3.16 (c)-(d) show the tuning of I-V characteristics by applying strain and laser at the same time.

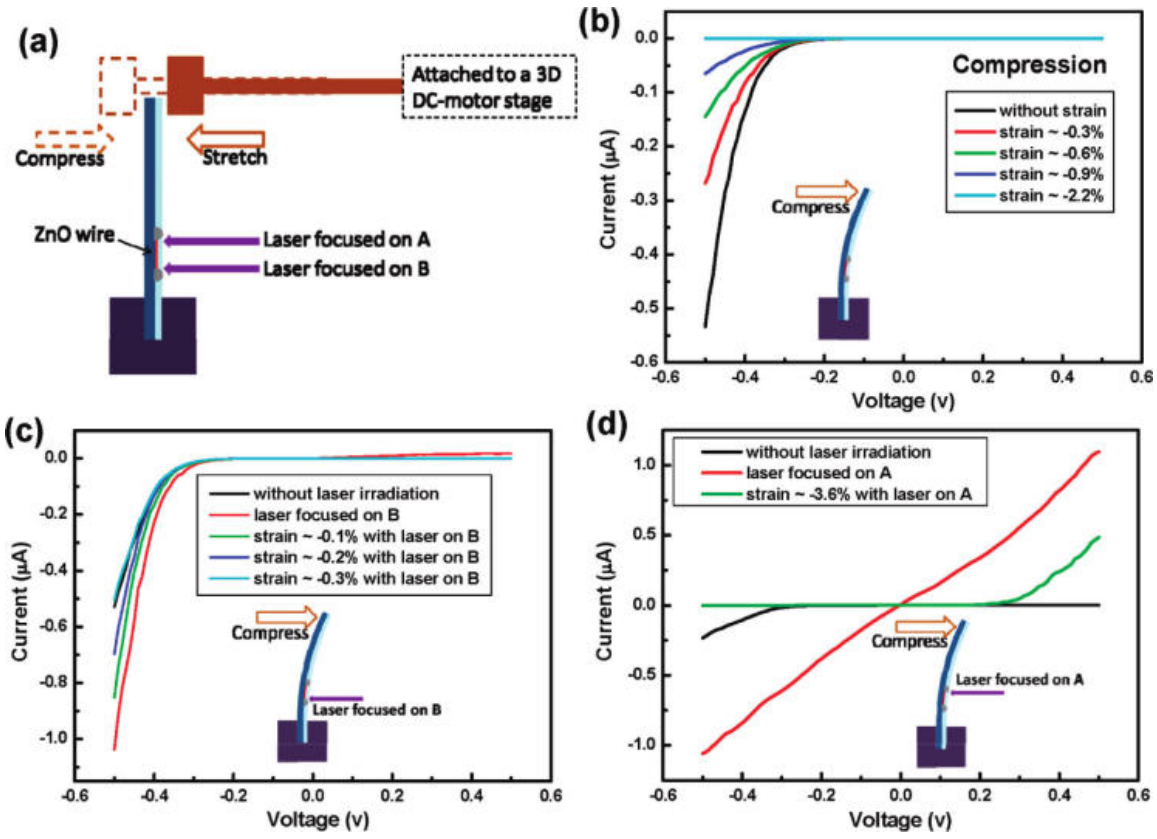


Figure 3.16 (a) Measurement set-up of the piezophototronic effect (b) effect of strain on a ZnO microwire device and (c) and (d) effect of strain coupled with photoexcitation at two positions [72]

Based on the same principle, the output of a ZnO microwire photocell was demonstrated to be strain-tunable [9]. Shown in figure 3.17 (a) is the piezoresponse of the single microwire device and figure 3.17 (b) shows the output current measured at zero bias as the laser point focused on different positions on the microwire. The photocurrent exhibited opposite polarities, which was attributed to opposite local electric field direction of the back-to-back Schottky barrier. The output current was shown to be tuned

by strain and the mechanism was again attributed to the tuning of the effective Schottky barrier height by the strain applied.

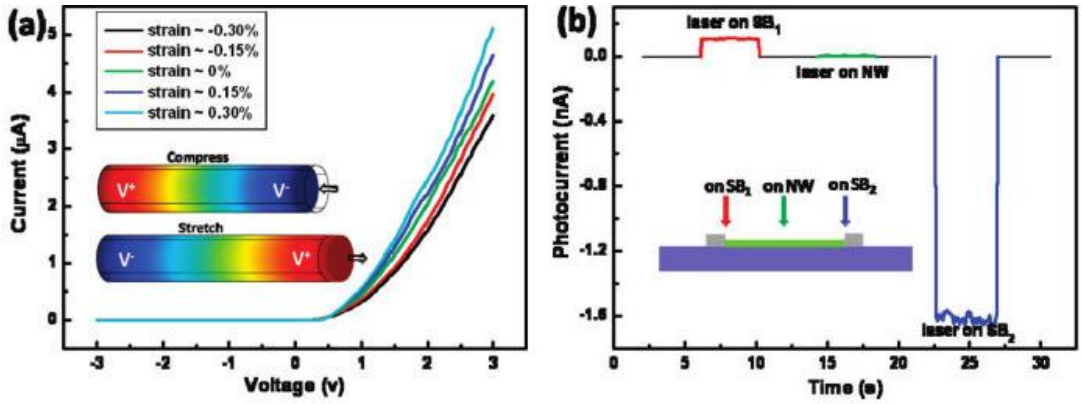


Figure 3.17 (a) Piezoresponse of a single ZnO microwire device and (b) Photocurrent measured by illumination on contacts and on microwire center [9]

3.2 Fabrication and Characterization of ZnO Microwire Photocells

3.2.1 ZnO Microwire Growth

ZnO microwires were grown by a high temperature evaporation method as indicated previously [73]. ZnO powder was placed at the center of the cylindrical chamber in the tube furnace, and an alumina plate was placed downstream. The furnace was heated to 1400℃ for 2 hours and the end product on the alumina plate was collected after the furnace cooled down. The resulting wires have a typical diameter of 2-10 μm and lengths that range from several hundred microns to several millimeters, with the c-axis as the wire axis.

3.2.2 Single Wire Photocell Fabrication

Single wire photocell was fabricated on a polystyrene (PS) substrate. The ZnO microwire was first laid down on the substrate and manipulated to the desired position, and then

silver paste (Ted Pella) was applied to fix its ends. The devices were left in air for at least 5 hours to allow complete drying of the solvent in the silver paste.

3.2.3 Characterization of the Electrical Properties and UV response of ZnO Photocell

The electrical measurements were done by a Keithley 4200 semiconductor characterization system.

A 325.0 nm He-Cd laser (KIMMON Koha Model IK5751I-G) was used as the light source to test the UV response of the ZnO microwires. The photon energy corresponding to this wavelength is 3.815 eV. The output power of the laser is 30mW and the output light polarization direction is vertical. The laser was directed and focused to the sample surface by a series of optics, as shown in figure 3.18. The output laser first goes through a variable ND filter (F1 in figure 3.18), which can be used to tune the transmitted light intensity. A mirror (M1) then directs the laser beam through two convex lenses (L1 and L2) whose focal point overlaps, which ensures that the output beam consists of parallel light. The light then goes through a beam splitter (M2). The whole system is fixed on an optical table for stability. 50% of the laser beam is then directed to a half wave plate (P), through the rotation of which the polarization of the light can be changed. A focusing lens (L3) then focuses the beam to a small laser spot where the device lies. Conversely, the light at the sample can return to the beam splitter (M2) and go through a bandpass filter (F2) where wavelengths of 325±2nm were filtered to ensure proper imaging on the CCD. Then the beam is directed by another mirror (M3) and focused by a convex lens (L4) before it reaches the CCD to form an optical image.

Two magnifications of the focusing lens (L3) were used: 10X and 40X. The difference in magnification not only affects the optical image that the CCD camera takes, but also

affects the area of the laser spot that hits the sample. For 10X magnification, a large laser spot with a diffused boundary is produced. For 40X magnification, a small laser spot with the diameter of approximately 10μm is produced, but even in this case the laser illumination area is not well-defined.

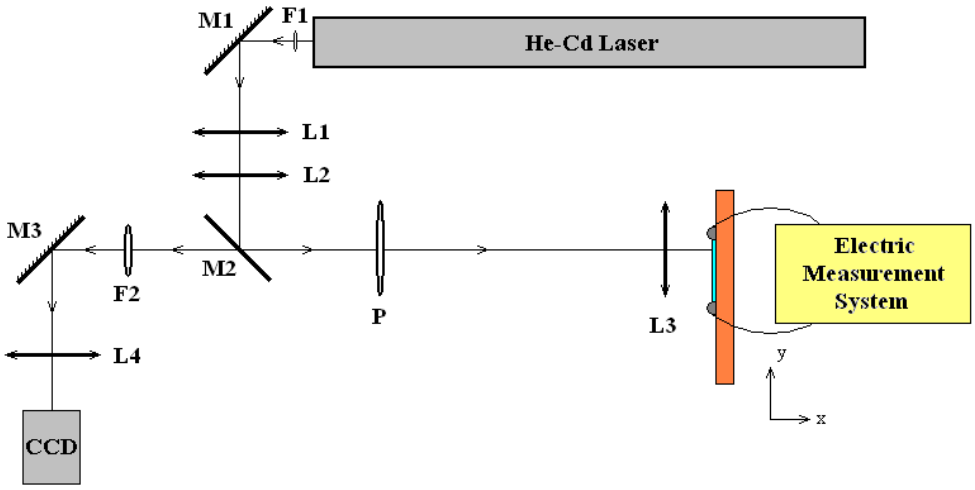


Figure 3.18 Measurement set-up for ZnO microwire photocells

The microwire photocell device is fixed on a 3-D stage that can be moved in both x and y directions with precision. The minimum step size for both x and y direction movement is 10μm.

During the measurements, the position of the laser illumination is switched with an increment of 10μm or 20μm. At each position, the response of the microwire to both horizontal polarization (indicated by h) and vertical polarization (indicated by v) was measured without touching the 3-D stage. The h and v polarizations are defined with respect to the surface of the optical table. For each type of polarization, the laser is periodically blocked to record the response for several on-off cycles. Three to five measurements are repeated and the final results are averaged to properly reflect the property of the microwire.

3.2.4 Results and Discussions

3.2.4.1 UV Response of ZnO Microwire Photocell with a Large Illuminated Area

UV response of the ZnO microwire device was first studied with 10X magnification focusing lens, which produces a large laser spot. The optical image of the microwire taken by the CCD camera is shown in figure 3.19. The wire diameter is around 10μm. Where the laser hits the wire, a light spot was produced on the CCD image due to photoluminescence, which has a size much larger than the actual illumination area.

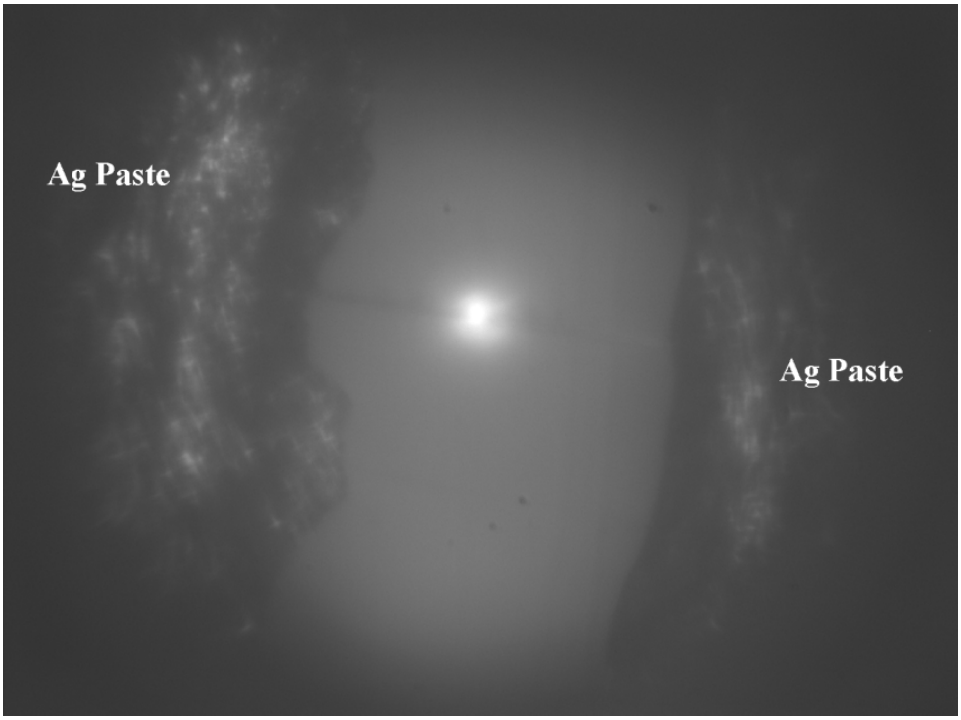


Figure 3.19 Optical image of the ZnO microwire under illumination acquired by CCD

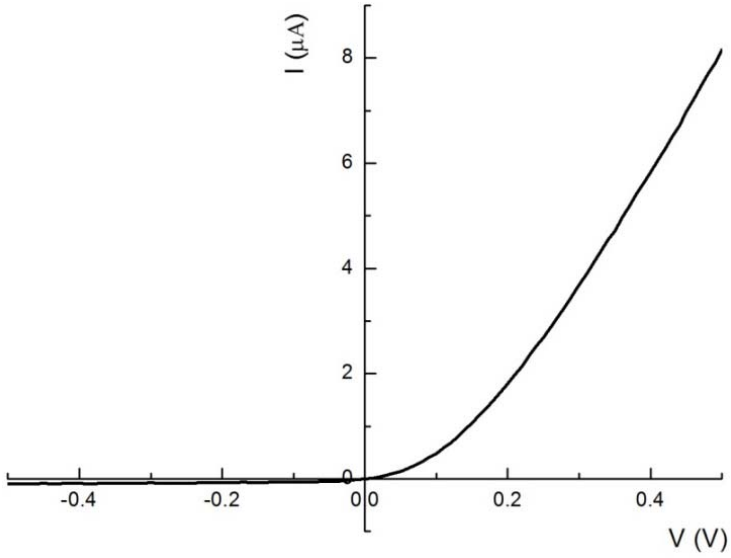


Figure 3.20 I-V characteristics of the ZnO microwire

Prior to laser illumination, the I-V characteristics of the ZnO microwire devices were tested. The result for the device is shown in figure 3.20. The I-V curve is non-linear due to non-symmetrical electrical contacts at the two ends of the nanowire, resulting in different Schottky barrier heights.

Effect of Illumination Position

The typical UV response when the laser shines on one end of the microwire is shown in figure 3.21. An average of approximately -6.5 nA of current is produced upon vertically polarized laser illumination and -7 nA upon horizontally polarized laser illumination.

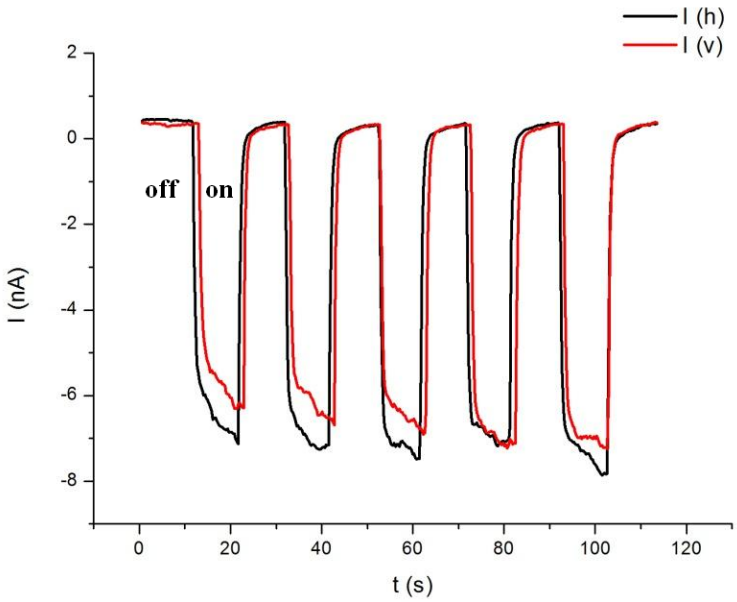


Figure 3.21 Current measured on ZnO microwire at zero bias upon UV illumination at one end

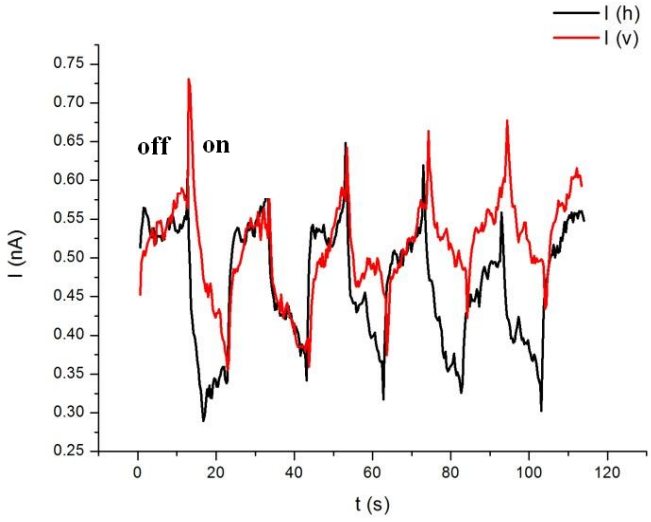


Figure 3.22 Current measured on ZnO microwire at zero bias upon UV illumination in the middle of the microwire

As the laser spot was moved towards the other end, the magnitude of this current gradually decreases, until at a certain point, the current drops to nearly zero, as shown in figure 3.22.

As the laser spot continues to move towards the other end of the microwire, the current switched polarity and become positive. The magnitude of the current increases as the laser spot was moved to the other end, and reaches maximum at the end, as shown in figure 3.23.

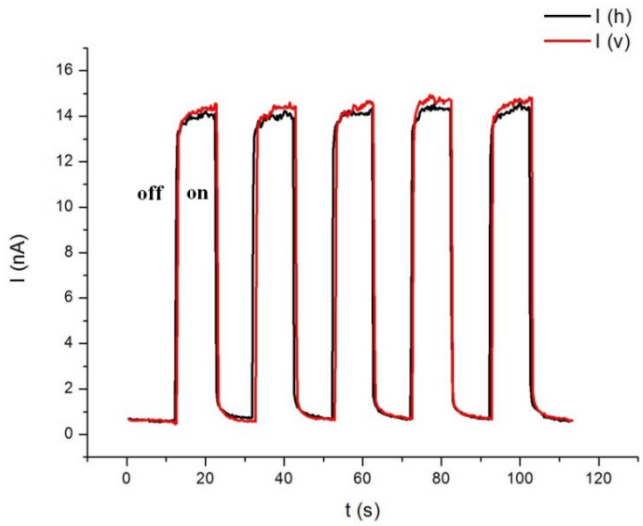


Figure 3.23 Current measured on ZnO microwire at zero bias upon UV illumination at the other end

The current response upon laser illumination on the microwire for horizontal and vertical polarizations as a function of laser illumination position is illustrated in figure 3.24.

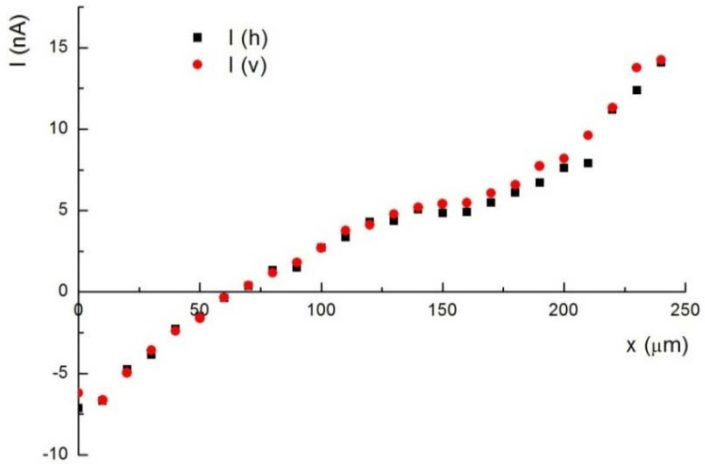


Figure 3.24 The current response of ZnO microwire as a function of illumination positions

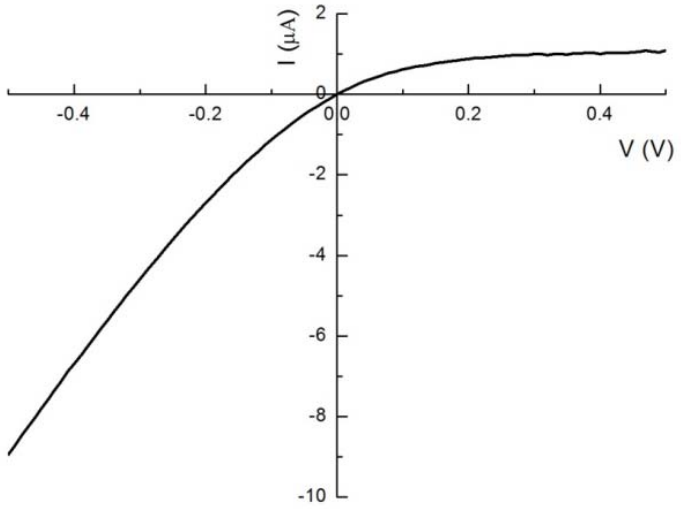


Figure 3.25 I-V characteristics of the ZnO microwire when polarity is switched

The polarity of the device is then switched by switching the electrical contact to the measurement system, and similar measurements were carried out on the same microwire device. The resulting I-V characteristics and UV response as a function of illumination positions are shown in figure 3.25 and 3.26, respectively. The direction of the current has switched polarity in this case, indicating that the measured current is truly due to the voltage drop induced by laser illumination rather than noise of the measurement system.

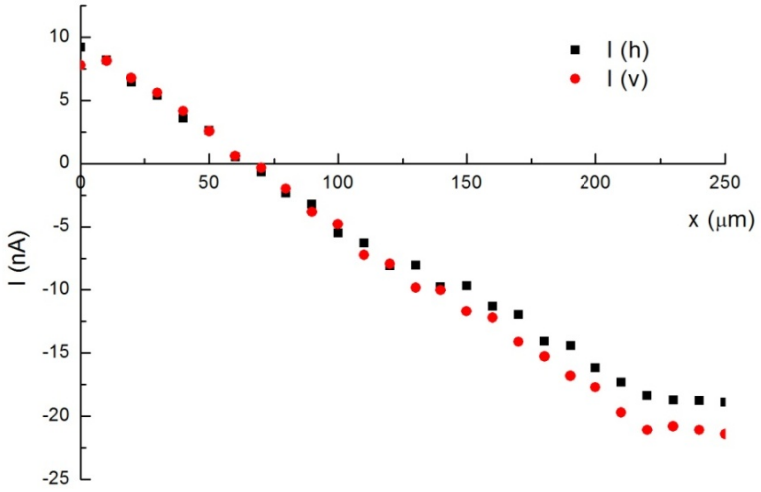


Figure 3.26 The current response of ZnO microwire as a function of illumination positions when polarity is switched

Effect of Illumination Intensity

The current response upon laser illumination at one position was measured at different laser intensities by adjusting the intensity filter near the laser output window and the resulting current as a function of normalized intensity is shown in figure 3.27.

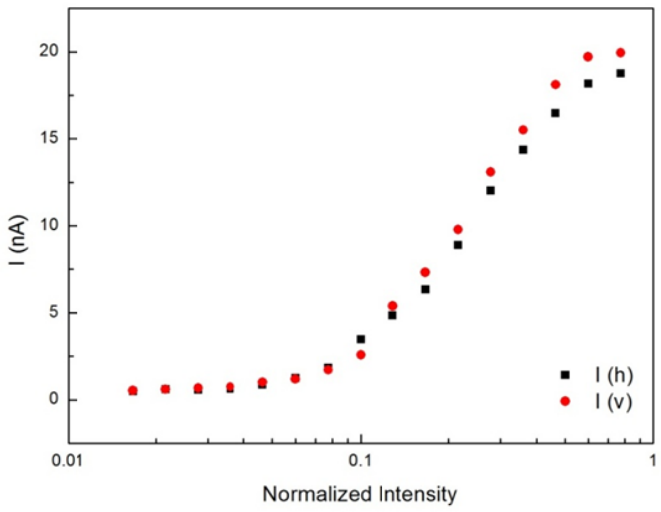
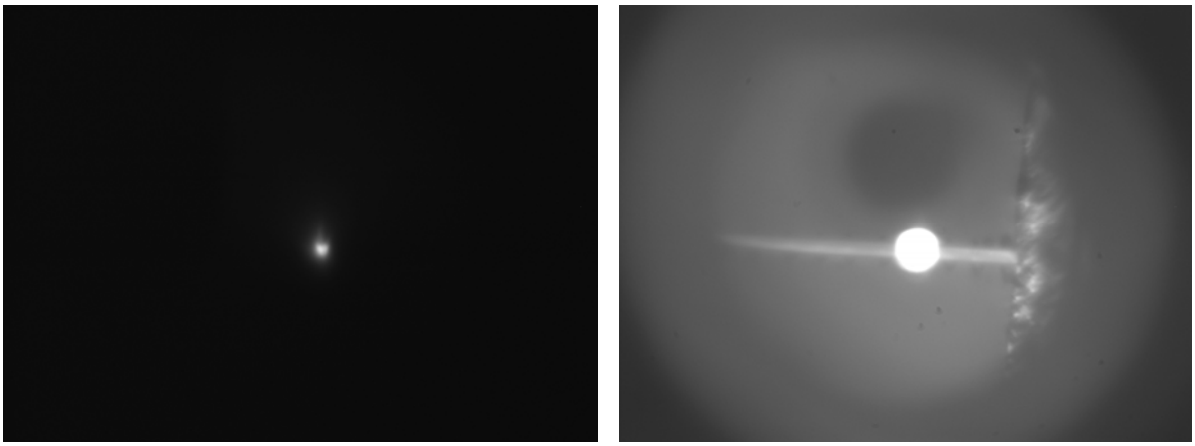


Figure 3.27 Current response as a function of normalized intensity for a ZnO microwire

3.2.4.2 UV Response of ZnO Microwire Photocell with a Small Illuminated Area

It is speculated that with the 10X magnification focusing lens, the boundary of the laser spot is not clear-cut and it is hard to define the illuminated area. A 40X magnification focusing lens was therefore used to test the sample.

Figure 3.28 (a) shows the optical image of the laser spot and figure 3.28 (b) is the sample image taken by the CCD camera with 40X focusing lens.



(a) (b)

Figure 3.28 Optical image of (a) the laser spot and (b) the laser illuminated nanowires with 50X focusing lens

The measured I-V characteristics for the sample are shown in figure 3.29. And the current response to small area UV illumination as a function of illumination position is plotted in figure 3.30.

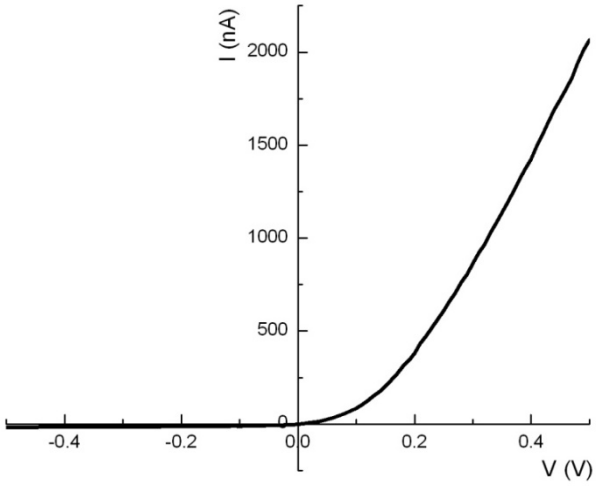


Figure 3.29 I-V characteristics of the ZnO microwire

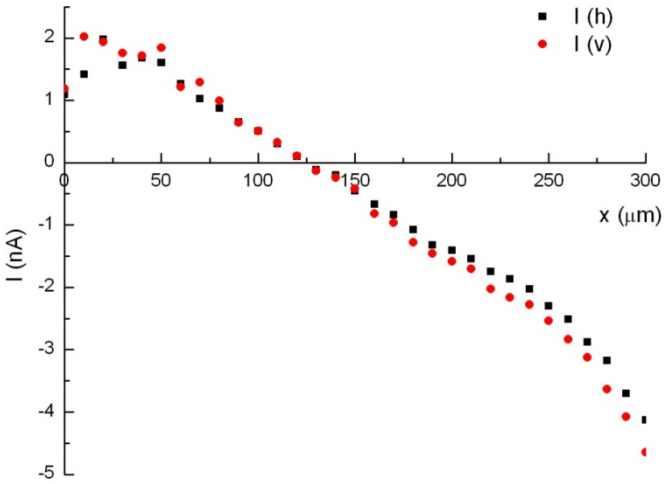


Figure 3.30 The current response of ZnO microwire as a function of illumination positions with a small illumination area

Two trends can be observed from figure 3.30:

(1) The point at which the current drops to zero does not occur at the center of the microwire.

(2) At most positions, the photocurrent for v polarization is higher than that for h polarization, though the difference is not significant.

For (1), two possible scenarios that can lead to the photocurrent profile with respect to illumination position are:

(A) Opposite Photocurrents

The laser illumination in this case has a profile that is not clear-cut, so that some light is on the wire ends even though the laser spot center is not. The local electrical field near the Schottky contact causes the photogenerated electron-hole to separate and produces a photocurrent. The photocurrents produced by the two junctions are of the opposite direction since the electric fields are opposite. The total current is the sum of the two opposite currents, which is dominated by one junction or the other except for at the zero point. Ideally, if the two junctions were identical, the zero point should lie in the center of the microwire. In reality, however, the magnitudes of the two currents are not the same due to the non-symmetry of the contacts as well as the difference in the light intensity that they get. Therefore the zero point usually does not lie in the center.

(B) Opposite Thermoelectric Currents

The laser spot can heat up the microwire, inducing a stable thermal gradient at steady state. In fact, when the laser spot hits on the wire body, the temperature gradients at the two junctions are of opposite directions, resulting in two thermoelectric currents of opposite directions. The total current is the sum of the two opposite currents, which is dominated by one junction or the other except for at the zero point. The Seebeck coefficient for ZnO microwires has not been reported, but the bulk value of -300μV/K is a good estimation [55], and thus the thermoelectric effect cannot be neglected.

For (2), there are possibilities that the half wave plate may have slightly different

absorption when rotated, yielding slightly different light intensity for different polarized light. However, if such experimental errors due to the equipment can be excluded, there are still two possible scenarios that may lead to the photocurrent difference for different polarizations:

(A) The absorption for polarized light for thin wires is dependent on the wire geometry. The magnitude of the electric field in the electromagnetic wave tends to be suppressed by the wire geometry when it is perpendicular to the wire axis. However, this effect only takes place when the wire diameter is significantly smaller than the wavelength of the light [56], whereas in the present study, the wire diameter of 10μm is much larger than the wavelength (325nm). Also, if the absorption in this experiment is dependent on wire geometry, the resulting current from v polarization should be lower than that from h polarization, which contradicts the experimental results. Therefore, it is very unlikely that this is the case in the present study.

(B) The absorption for polarized light is dependent on the anisotropy of the crystal structure. In particular, ZnO nanowires grow in the c-axis direction. For ZnO, the refractive index, n and the absorption coefficient, α are different for polarizations that have different angles between the electric field and the c-axis. The difference has not been reported for nanomaterials, but since the microwire is thick compared to the wavelength as stated above, we hereby treat the material using the bulk values.

Consider an incident light beam I that is normal to the air/microwire interface, as illustrated in figure 3.31. The light beam is first incident on the front surface, where a portion of light R_1 is reflected and T_1 is transmitted. The transmitted light then travels inside the microwire and gets attenuated, and is then incident on the back surface, where a portion of light R_2 is reflected. We only consider the first two reflections since after reflection once at the back surface the light intensity that still remains in the wire is

negligible.

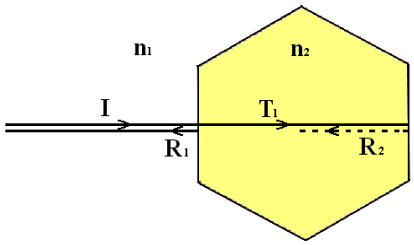


Figure 3.31 Simplified cross section model for light reflection and absorption in the nanowire

From Fresnel equations, the reflection and transmission coefficients for normal incidence are given by

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \quad (1)$$

$$T = 1 - R \quad (2)$$

where R is the reflection coefficient, T is the transmission coefficient, and n_1 and n_2 are the refractive index of air and ZnO, respectively.

The absorption of the light in the wire is determined by the Beer-Lambert Law:

$$I = I_0 e^{-\alpha x} \quad (3)$$

where I_0 is the intensity of incidence, I is the light intensity transmitted through thickness x, and α is the absorption coefficient.

The reflective index for air n_1 is 1.0. The value reflective index for ZnO, n_2, equals ~1.9 when the polarization is perpendicular to c-axis and ~2.0 when the polarization is parallel to c-axis. The absorption coefficient, α, equals $2.00\times10^{-5}cm^{-1}$ when the polarization is perpendicular to c-axis and $2.19\times10^{-5}cm^{-1}$ when the polarization is parallel to c-axis [57]. For the absorption thickness, the wire diameter of 10μm is used. According to equations

(1)-(3), the absorbed light for perpendicular polarization with respect to the c-axis is 91.28%, while the value for parallel polarization is 89.12%. Therefore, in this study, the fact that v polarization induces higher current than the h polarization may be attributed to the anisotropy of the ZnO crystal structure.

Effect of Illumination Intensity

The current response as a function of positions was tested under different laser power. The result is plotted in figure 3.32.

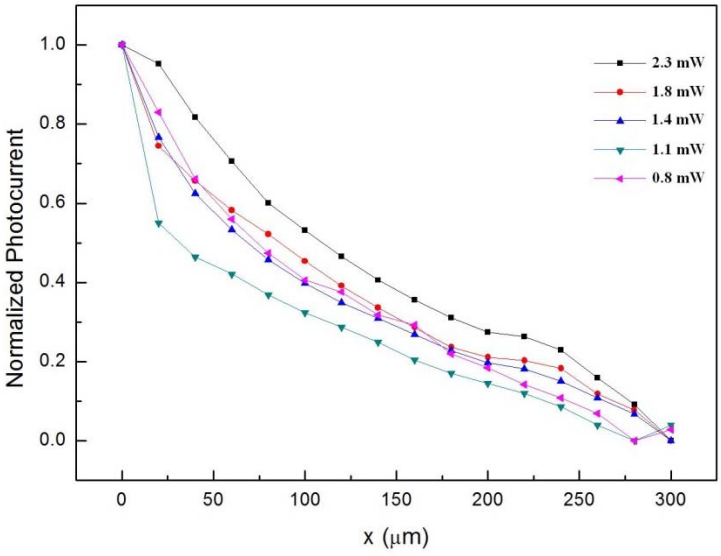


Figure 3.32 The current response of ZnO microwire under different laser power

Influence of Thermoelectric Effect

To evaluate the influence of thermoelectric effect on the measured current upon laser illumination, a single microwire device with two Ohmic contacts was fabricated with In-Ga alloy and silver paste. Figure 3.33 shows the I-V characteristics of the device. The I-V curve is linear, demonstrating good Ohmic contact. The conductivity for the Ohmic contacted sample is much higher than that of Schottky contacted ones.

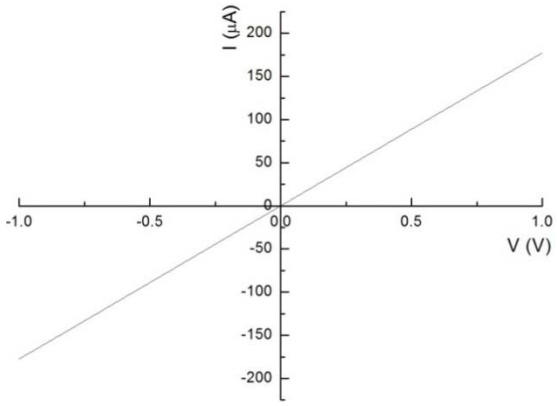
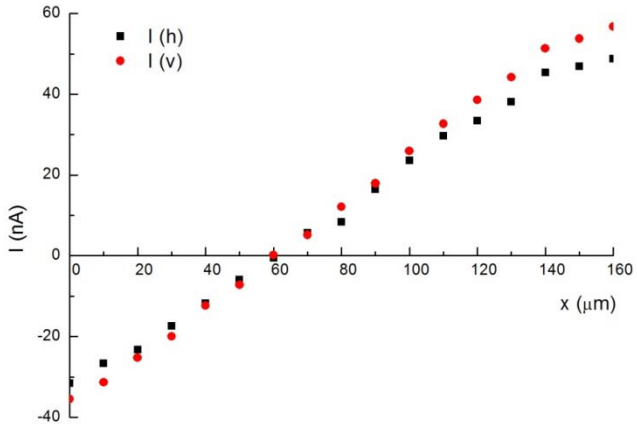
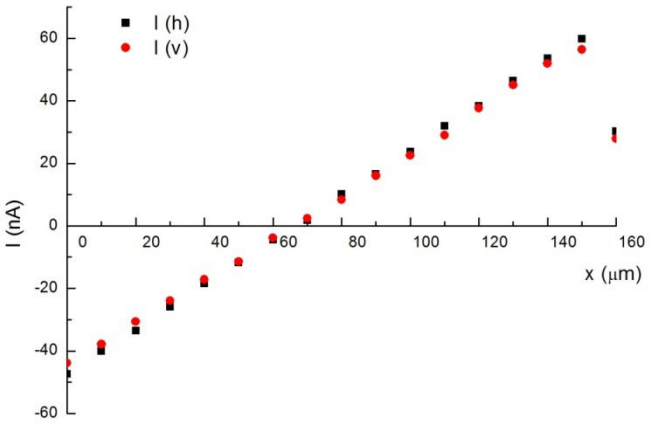


Figure 3.33 I-V characteristics of a ZnO microwire with two Ohmic contacts



(a)



(b)

Figure 3.34 Current response upon UV illumination for (a) horizontally and (b) vertically placed ZnO microwire

The measured current for the Ohmic contact sample is shown in figure 3.34. To confirm that the current difference is due to polarization switch rather than other factors, apart from the measurements carried out with the microwire placed horizontally as in previous studies, additional measurements with the microwire placed vertically was done. Figure 3.34 (a) is the current measured when the wire is placed horizontally, so that the h polarization is the polarization parallel to the wire axis; figure 3.34 (b) shows the current measured when the wire is placed vertically, and the h polarization is the polarization normal to the wire axis.

Four observations can be made from figure 3.34:

(1) The current for Ohmic contacted device is not zero, and follow a similar trend in which the total current switches sign as the illumination position changes. Therefore it is very likely that in the previous tests with Schottky contacted devices, not all the current is a result of the local electric field near the Schottky contacts. Note, however, that the resistivity of the Schottky contacted device is much higher, and therefore the influence of the thermoelectric potential should be smaller. It is hard to quantitatively evaluate the magnitude of thermoelectric component of the current in the Schottky devices.

(2) The current for Ohmic contacted device exhibit an almost linear relationship with respect to the illumination position. This is expected for thermoelectric current assuming that the temperature gradient at steady state is constant.

(3) The zero current point for the thermoelectric current is not at the center of the microwire. This may be attributed to the non-symmetrical contacts at the wire ends. Even though the non-symmetry effect does not affect the I-V curve, it is very likely that the two ends have different thermal resistance, resulting in a non-symmetrical thermal gradient.

(4) Regardless of the direction in which the microwire is placed, the current is always higher for the polarization perpendicular to the wire axis (c-axis), and is always lower for the polarization parallel to it. This again can be attributed to the difference of absorption due to crystal structure anisotropy.

3.3 Fabrication and Characterization of GaN Nanowire Devices

3.3.1 GaN NW Growth

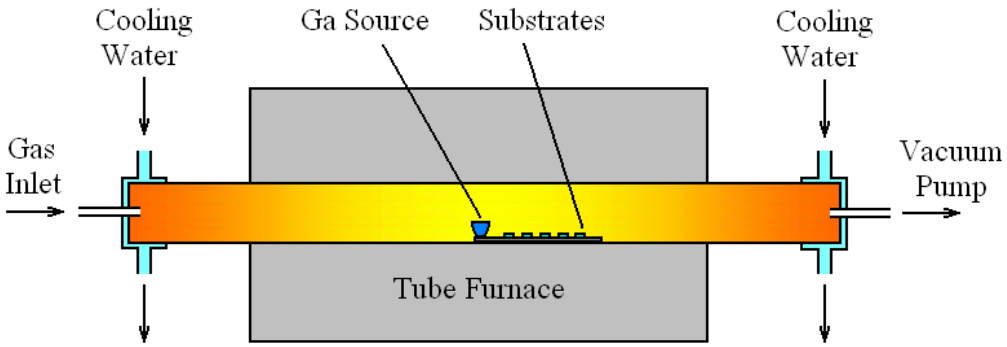


Figure 3.35 Set-up for GaN nanowire growth

GaN nanowires were synthesized by vapor phase method in a tube furnace. Single crystalline r-sapphire and epitaxial c-GaN on c-sapphire wafers were used as the substrates. First, the substrate is cleaved into 4mm×4mm pieces, and after that the catalyst material was deposited on the substrates. Ni was used due to its compatibility with GaN material [2]. The Ni catalyst deposition was done by two methods: (1) direct sputtering of a 2 nm Ni thin film, and (2) dip coating of 0.005 mol/L $Ni(NO_3)_2$ solution in ethanol twice. Five substrates were then placed on an alumina boat with a interspacing of approximately 1 inch. Ga pieces (Alfa Aesar, 99.99%) were used as the Gallium source. The source was placed in an alumina crucible, which was then put at the end of the boat on which the substrates were placed. The boat was then inserted into the furnace tube

such that the source sits at the center of the furnace where temperature is the highest and the substrates are in the downstream position when the gas was fed. Figure 3.35 shows the configuration inside the furnace.

The furnace tube is then pumped down to a base pressure of 10 mT for several hours to evacuate residual oxygen. Then NH_3 of the flow rate 30 sccm was fed through the gas inlet and the pressure inside the tube was adjusted to 3-10 T. After that, the cooling water supply was turned on. The furnace was heated to 800℃ at a ramp rate of 30℃/min and kept for 30 min to anneal the catalyst, and then the temperature was raised to 1000℃ at the same ramp rate and kept for 30-60 min. The furnace was then cooled down to room temperature without turning the NH_3 supply off. The nanowires were collected on the substrates.

3.3.2 Single Nanowire Device Fabrication

Single wire devices were fabricated on polystyrene (PS) substrates which are typically 32mm long, 7mm wide and 1mm thick. The GaN nanowire was first laid down on the substrate and manipulated to the desired position under an optical microscope, and then silver paste (Ted Pella) was applied to fix its ends. Extreme caution was taken to make sure the contacts do not short due to the small wire length. The devices were left in air for at least 5 hours to allow complete drying of the solvent in the silver paste.

3.3.3 Characterization of GaN Nanowires

3.3.3.1 Scanning Electron Microscopy (SEM)

A LEO 1530 SEM was used to record the morphology of the grown nanowires. An acceleration voltage of 7 kV was used.

3.3.3.2 Characterization of the Electrical Properties of GaN Nanowire Devices

The electrical measurements were done by a Keithley 4200 semiconductor characterization system. To test the effect of strain on the transport properties of the device, the PS substrate was fixed at one end and strain was applied by a motion controller (Newport ESP300) at the other end, while the electrical properties were measured.

3.3.4 Results and Discussions

The five substrate positions were denoted by #1-5, respectively, starting from the position that is nearest to the Ga source.

Figure 3.36 shows a typical SEM image of the as grown GaN nanowires on c-GaN substrates on substrate position #4. The diameter of the fabricated nanowire is 50-200 nm, and the length is 10-20μm. Figure 3.37 is the EDS spectra which have confirmed the composition to be Ga and N.

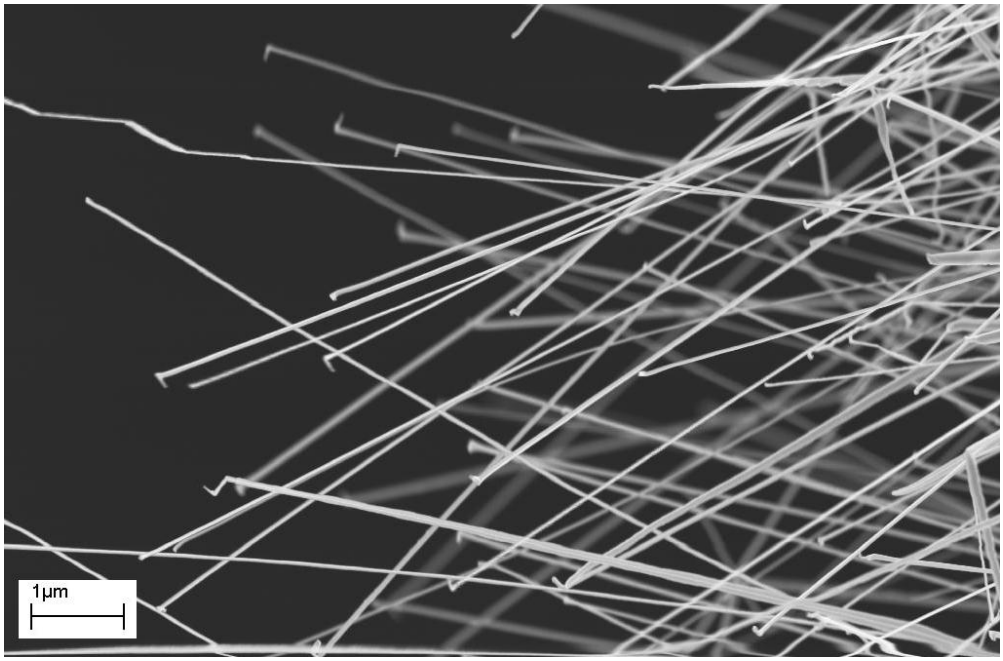


Figure 3.36 SEM image of as grown GaN nanowires on c-GaN position #4

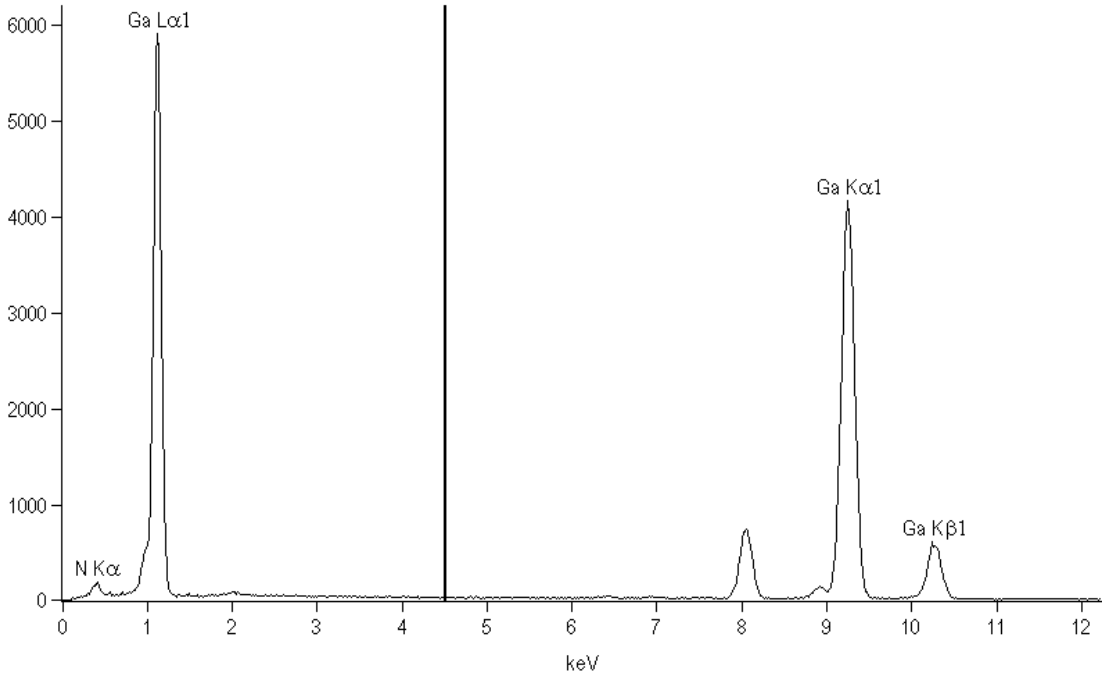


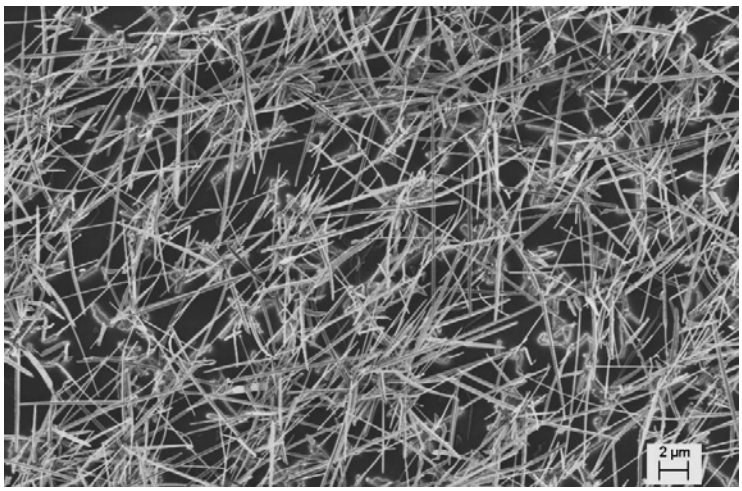
Figure 3.37 EDS spectra on a single GaN nanowire

Different from previously reported CVD growth on Si, SiO_2, Si_3N_4, sapphire, and a-GaN [74-76], the GaN nanowire grown in this study employed c-GaN substrate, and compared the growth morphology with those grown on r-sapphire substrates under the same conditions. A lot of growth studies used Ga_2O_3 as the Ga source [77, 78], while Ga was used in this study. Moreover, c-GaN was used as substrate by Huang *et. al* [12], however the catalyst in their work was deposited by sputtering of Ni film solely, while in this study, both Ni sputtering and $Ni(NO_3)_2$ solution coating was employed.

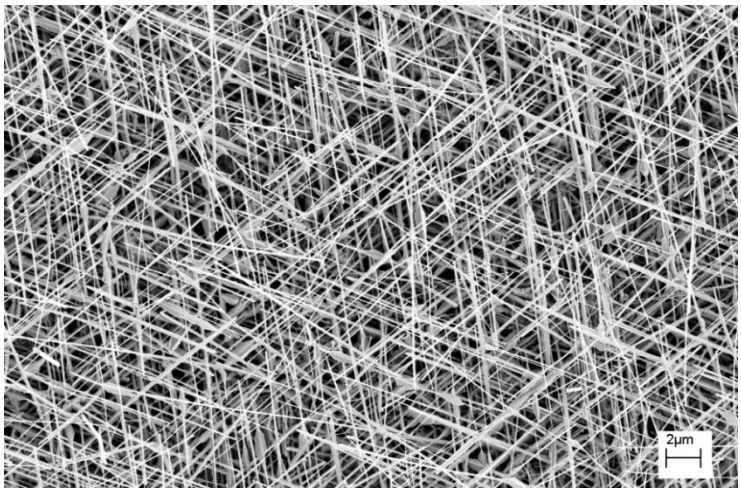
3.3.4.1 Effect of Substrate Material

Figure 3.38 (a) shows a typical SEM image of GaN nanowires grown on r-sapphire at a growth pressure of 5 T and figure 3.38 (b) is the image of GaN nanowires grown on GaN substrate under the same condition. The nanowires grown on sapphire substrate showed

no orientation preference and the wire density is relatively lower. Nanowires grown on GaN substrate, on the other hand, exhibited three preferred orientations that are separated by an angle of approximately 120°, and the wire density is apparently higher, with a slightly larger length as well.



(a)

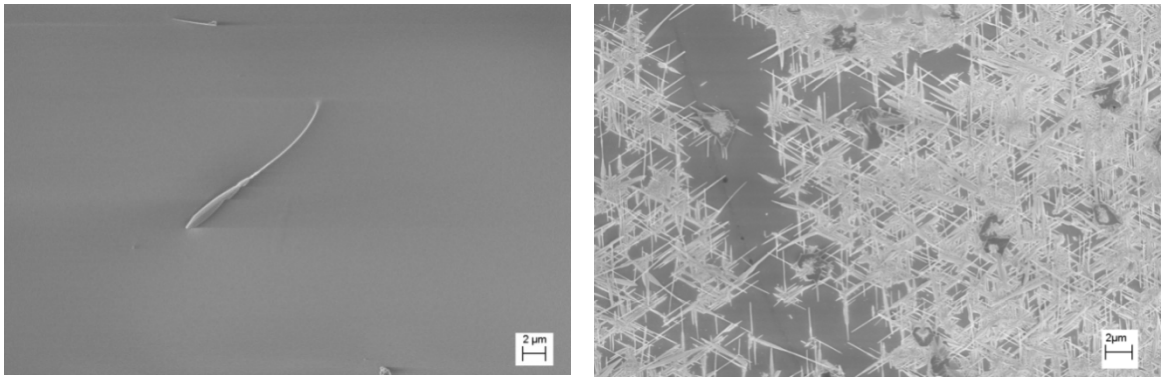


(b)

Figure 3.38 GaN nanowires grown on (a) r-sapphire and (b) c-GaN under similar conditions

The difference can be explained by the different growth surface on the two substrates. Further comparison of the two substrates on which nanowire growth are sparse, in figure

3.39 (a) and (b), shows that on sapphire substrates, the area underneath the nanowire is very clean, while on GaN substrates, a rough film was deposited. Therefore, GaN nanowire growth on sapphire takes place by direct nucleation on the sapphire surface, while the growth on GaN involves an in-situ deposition of GaN islands prior to the nanowire nucleation, and the nanowires are grown on the deposited GaN islands.



(a) (b)

Figure 3.39 Sparse nanowires grown on (a) r-sapphire and (b) c-GaN

It is therefore inferred that the slightly larger lattice mismatch of GaN with sapphire increased the interfacial energy and decreased the nucleation density. Also, for GaN nanowire grown on GaN substrates, the orientation of the underlying islands may have transferred the crystallographic orientation preference to the nanowire, resulting in the regular geometric configuration. Thus all the following discussions are on growth on GaN substrates.

3.3.4.2 Effect of Substrate Position

The main differences between the five positions are temperature and source concentration. The effects of growth temperature and source concentration are therefore studied in combination by comparing the growth that occurred at the five positions.

Figure 3.40 (a)-(e) show the growth on substrates # 1-5, respectively, at a growth pressure of 5T with $Ni(NO_3)_2$ solution as the catalyst. Figure 3.40 (f)-(h) show the growth on substrates # 1-5 grown under similar conditions, with sputtered Ni thin film as the catalyst.

It can be seen from figure 3.40 that, regardless of the catalyst, the effect of substrate is similar. For positions #1 and #2, nanowire growth is mostly suppressed by film deposition. From positions 3-5, thin nanowires are grown with increasing density and decreasing width.

The effect of substrate position can possibly be explained by the competition of film growth and nanowire growth kinetics.

According to the classical nucleation theory, the driving force for nucleation is super-cooling. At high temperatures, nucleation is harder due to a lower driving force, and so new adatoms like to stick together since adsorption onto an atomic step can reduce the interfacial energy dramatically. The islands formed during the initial stage are therefore quickly connected to form a film. Also, the source atoms tends to be deposited on the nanowire sidewalls, which lead to very thick and conical nanowires, as shown in figure 3.40 (a) and (b). Moreover, at high temperatures, the catalyst particles are harder to reach supersaturation, resulting in slow nanowire growth. Therefore, thin film formation is favored in this case.

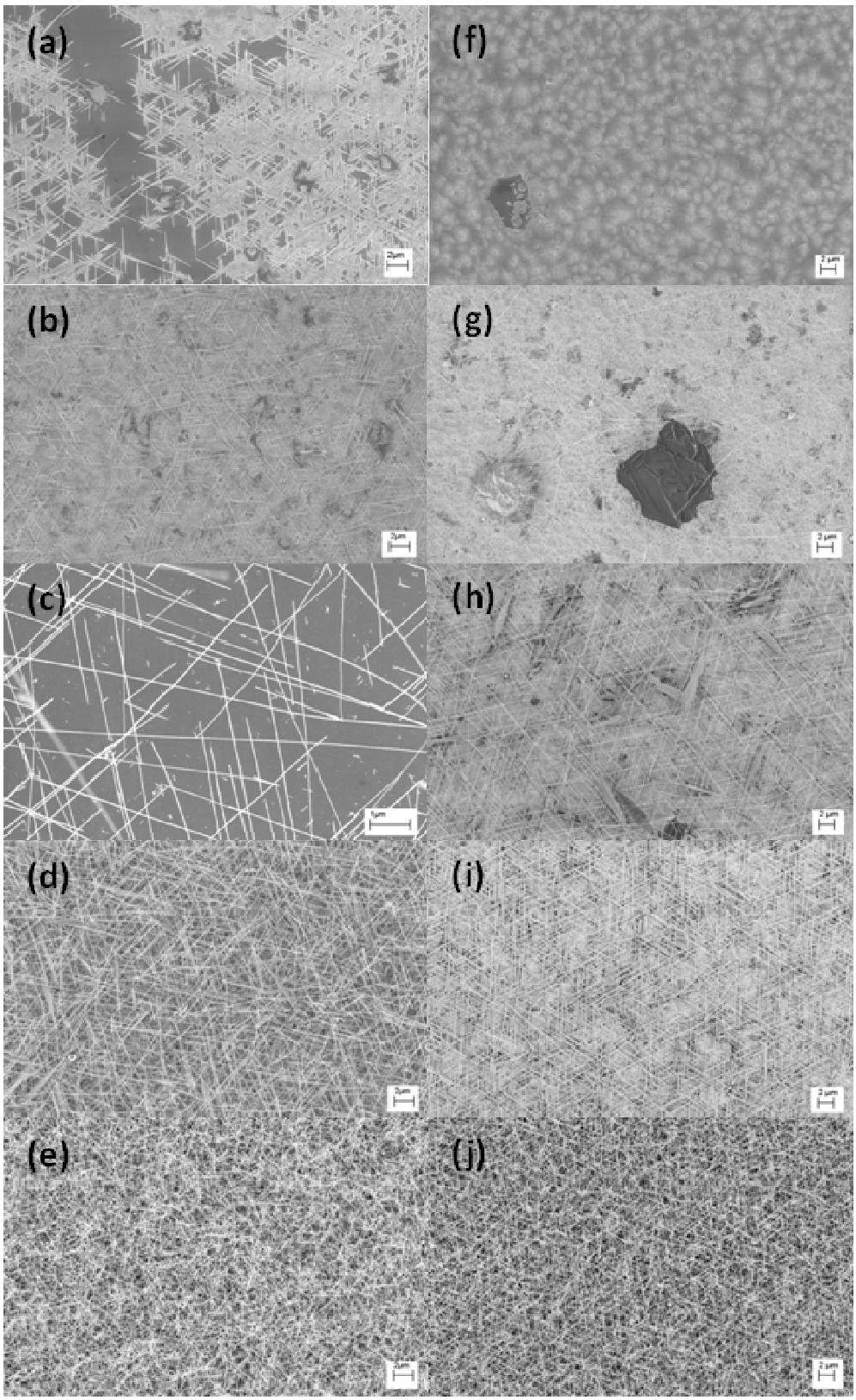


Figure 3.40 GaN growth on substrates # 1-5, with (a)-(e) $Ni(NO3)_2$ solution as the catalyst and (f)-(h) with sputtered Ni thin film as catalyst

At low temperatures, however, nucleation is easier, and islands tend to remain unconnected. The source atoms do not tend to deposit on sidewalls, and since the catalyst particles can easily reach supersaturation, and nanowire growth is fast, which results in long and uniform nanowires. In figure 3.40 (c), it is obvious that a great portion of catalyst particles did not result in nanowire growth. This means that these catalyst particles in this case did not reach supersaturation. As the temperature is further lowered as in figure 3.40 (d)-(e), more catalyst particles could reach supersaturation and the resulting nanowire density is higher.

Note that the source vapor concentration at different substrate positions may be different and this will have an influence on the growth as well.

3.3.4.3 Effect of strain on transport characteristics of GaN nanowires

Figure 3.41 is the acquired optical image with the same set-up as in section 3.2 with a 40X focusing lens. The distance between the two silver electrodes is approximately 10 μm. The GaN nanowires exhibits strain-sensitive behavior, and can be potentially used for a strain sensor. Figure 3.42 (a) shows the I-V response of two GaN nanowire devices to compressive strain.

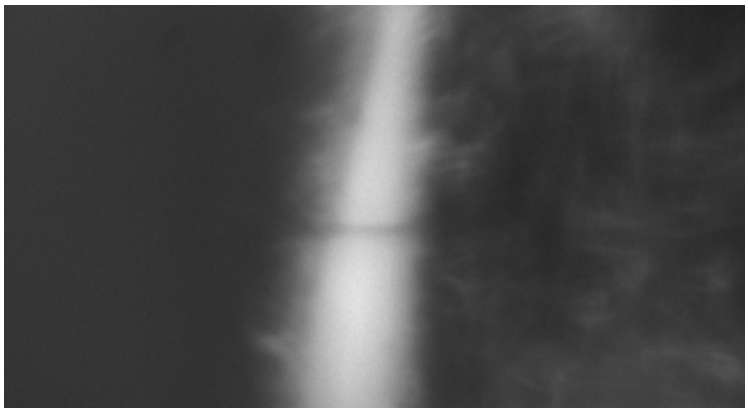


Figure 3.41 40X Optical image of the GaN nanowire between Ag electrodes

The electrical response can be explained by the effect of piezopotential on the Schottky barrier height at the two contacts. The current transport is dominated by the Schottky barrier that is reverse biased which has a greater resistance. The original I-V curves in figure 3.42 indicated that for both devices, the Schottky barrier is higher at one end and lower at the other.

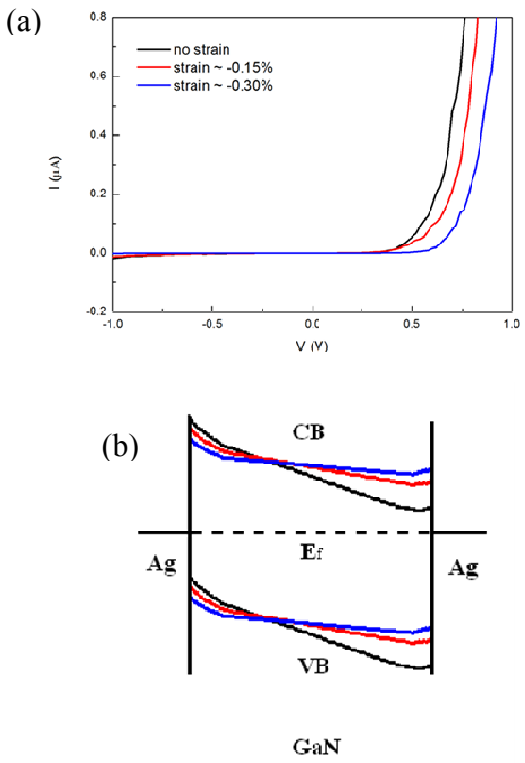


Figure 3.42 (a) and (b) response of two GaN nanowire devices under compressive strain; (c) and (d) corresponding band diagrams of the two devices

When strain is applied to a piezoelectric nanowire, the piezoelectric effect dictates that the piezopotential inside the crystal is negative along the polar axis, which raises the Schottky barrier, and positive on the other side, which decreases the Schottky barrier [11]. Previous simulation studies have shown this effect in GaN nanowires [2]. Note that the

positive piezopotential can be partially screened by the free electrons in the crystal and its effect is relatively lower than negative piezopotential. Therefore, two types of response to strain are present, depending on the polar axis direction of the nanowire. If the positive piezopotential is at the lower barrier side, then the barrier height change is as illustrated in figure 3.42 (b), which leads to the strain response in figure 3.42 (a).

3.4 Conclusions and Future Work

Single ZnO microwire photocell devices have been fabricated and their electrical response upon UV illumination at zero bias was examined. The current output switches polarity as the illuminated area scans through the whole microwire. This is attributed to the competition between the two opposite photocurrents and thermoelectric currents. And there is a null point on the nanowire where the two currents that are in the opposite directions cancel each other. The response also shows polarization dependence and this is explained by the different reflection and absorption at the ZnO/wire interface due to crystallographic anisotropy.

GaN nanowires were synthesized on r-sapphire and c-GaN substrates. The effect of substrate material and substrate position was qualitatively discussed. Electrical characterization of single GaN nanowire devices has also been carried out, and the strain response of these nanowire devices has been tested, which is the first report on GaN piezotronic devices. The influence of piezopotential on the transport properties was used to explain the observed I-V characteristic change.

Recommended future work includes:

(1) For ZnO microwire photocells, new experimental design should be taken to minimize or eliminate thermoelectric effect so that the UV response can be quantitatively characterized. For example, substrates with higher thermal conductivity can be used, or

the device can be actively cooled during laser illumination and measurement.

(2) For GaN nanowires, the device yield is relatively poor and device fabrication is very difficult due to its extremely short length. The short length also affected the possibilities to do further characterizations on the device. Therefore, it is recommended that further optimization of the growth process can be done to grow longer and more uniform nanowires.

CHAPTER 4

CONCLUSIONS

4.1 Comparison of Ceramic Thin Films and Nanowires for Piezoelectric Applications

4.1.1 Fabrication and Integration

The vapor phase fabrication techniques for nanowires, such as thermal evaporation, PLD, MOCVD and MBE can be similar to those utilized for thin films, since they all involve vapor transport to the desired growth area. Indeed, several of the current nanowire growth technologies are based on mature semiconductor thin film growth process. The major difference is that for nanowire growth, a catalyst, either foreign or intrinsic, is often used to break the symmetry and induce one dimensional growth.

To get high quality crystallized structure, piezoelectric thin films fabricated by these vapor phase methods typically require high deposition temperature, or high temperature post-annealing, which makes the process not compatible with current microelectronic technologies. The current solution is that to fabricate these thin films separately before they are integrated into the whole system, which dramatically increases the cost as well as limits the versatility of the technology. Moreover, unlike bulk piezoelectric ceramics that are typically based on flexible mechanical parts, piezoelectric thin films usually require a compliant substrate to which strain can be applied due to the large in-plane electromechanical coupling factors. And the high processing temperatures also prohibits the use of polymer substrates, which greatly limits the applications of such devices to a few inorganic flexible substrates such as MEMS cantilevers or ultrathin silicon wafers. The relative stiffness of such substrates may put some fundamental limitations on the

frequency at which the device works. It also does not allow much possibility to produce composite materials with soft materials as the matrix. However, the thin film processing technologies are currently in its mature phase and are already widely employed in the electronic industry. Therefore, thin film devices are simpler to manufacture and commercialize.

For nanowire growth by the vapor phase methods, the high temperature in the growth process can potentially impair the ability to be integrated into microelectronics in a similar manner. Therefore it is very likely that as nanotechnology enters the massive production phase, the growth process must be separated from microelectronic fabrication steps. However, the geometry and mechanical robustness of nanowires offers a variety of options to transfer to a substrate other than the rigid ones they are grown on. This provides more technical flexibility for low-cost integration with polymer substrates, synthesis of nanowire-polymer composites, and even possible integration with CMOS technology. The drawback of nanowire growth is, however, that the reproducibility of such processes is still a problem and extremely fine control of the growth environment is required as the ultra-small dimension of the nanomaterials also means that they are ultra-sensitive to small perturbations of the growth environment.

Fabrication of thin films and nanowires can both be achieved with solution synthesis techniques such as hydrothermal methods. For most piezoelectric thin films, however, the hydrothermally derived films are of inferior properties than those fabricated by vapor phase methods. The nucleation and growth process depends on the fluidics of the solution, and the as synthesized films are commonly not dense enough for electrical applications. Also, the incorporation of hydroxyl groups in the lattice often results in deteriorated leakage properties.

For nanowire, the hydrothermal method provides a low-cost, low temperature and highly reproducible synthesis route on large substrate areas and a variety of substrate materials. Although the electrical properties of the as-synthesized nanowire is somewhat inferior to those synthesized by vapor phase methods, the unique advantages offered by wet chemical method are still very attractive for potential industrial scale device technologies.

4.1.2 Yield

Since the thin film devices have a certain working area, the yield of such devices is determined by all the grains and, most importantly, all the grain boundaries that are covered by the electrode. As a result, any weak spots such as voids, pinholes, contaminated grain boundaries etc. can all serve as potential conductive paths that can lead to electrical shortage or breakdown. It is therefore very hard to achieve a high yield on large area devices with thin films; and once such failed devices are detected, it is very hard to rework on them and the defective ones have to be discarded.

On the contrary, the yield of nanowire devices is not so tricky since the devices are fabricated in large quantities at a time and tested on a one-to-one basis. The major problem that lowers the device yield is possible contact problems due to the small size of such structures, rather than intrinsic material defects.

Another major yield problem for piezoelectric thin films is cracking, which leads to electrical shortage and breakdown. Cracking greatly limits the process conditions and yield of the thin films. Little thermal expansion coefficient mismatches with the underlying layer may result in severe cracking of thin films during heat treatment. Therefore, careful substrate selection is required for thin film growth and subsequent heat process. Care should also be taken to optimize the heat treatment conditions since a high ramp rate can cause cracking too. The tendency to crack is intrinsic to the thin film

geometry and greatly limits their applications when stress needs to be applied. Nanowires obviously do not have this problem due to their standalone nature when synthesized, and usually the only factors that should be considered for nanowire growth is the crystal orientation and lattice mismatch.

4.1.3 Piezoelectric and Mechanical Properties

Geometrically, the structure of an oriented polycrystalline film can be seen as an ensemble of interconnected, extremely dense "nanowires", or columnar nanosized grains. The measured properties of the thin films are in fact the average properties of that ensemble of grains, and as a result, are more stable and reproducible. Nanowires, on the other hand, consists of only one single "grain" and dramatic difference can exist even between nanowires from the same batch, on the same sample. The process to efficiently distinguish nanowires with better properties from those with less desirable properties remains an open question as of today.

The same material often exhibits higher piezoelectric coefficient in their nanowire form than their thin film form. Theoretically, thin films have lower piezoelectric coefficients than the bulk, due to the clamping effect of the substrate. Also, thin films are prone to mechanical cracking and fatigue during their service period even with very small applied strain, while nanowires are more compliant and dislocation-free, and can stand up to 6% strain. Nanowires are therefore very promising material forms for piezoelectric applications. It is worth noting that fabrication of nanowire form of traditional high piezoelectric coefficient materials, such as PZT and Barium Titanate, is quite difficult and has only been achieved recently, which is far from mature.

4.1.4 Device Possibilities

Possible device structures for thin films are greatly limited by their geometry and process. Most of the current thin film deposition techniques are designed for a planar geometry, and as have been pointed out in Chapter 2, it is very difficult for thin films to be applied to 3-D surfaces. Material compatibility is another issue, and in particular, the ferroelectric materials which are widely used for their piezoelectric properties today put strict limitations to the electrode and barrier materials as stated in Chapter 2.

The nanowire geometry opens up a lot of potentially new device possibilities, for both nanowire arrays and single nanowire designs. And the ease to form composites with a soft material is a plus, especially for applications that require high electromechanical coupling. Moreover, as shown by the diverse applications of nanowires in Chapter 3, the coupling between piezoelectricity with other properties on the nanoscale has offered a lot of novel field to explore.

4.1.5 Toxicity

The environmental and health effects of piezoelectric materials have become a serious concern over the years. Traditional piezoelectric materials such as PZT and PMN contain lead and can have severe adverse effects on human health. Alternatively, lead-free materials such as Barium Titanate are developed, but their piezoelectric properties are inferior as well. The problem is more aggravated with the increasing need to develop implantable piezoelectricity-based devices, and the answer offered by current technologies is the utilization of hermetic sealing and packaging of such materials, which is not fail-safe and lacks biosafety testing standards.

In comparison, there are no toxicity issues with ZnO and GaN in their bulk form. When the material chemistry is considered, ZnO breaks down to biocompatible ions, and GaN is chemically stable. It is still controversial if the nanosized form of such materials is bio-

safe, although preliminary studies have shown promising results [79]. The bio-safety of nanomaterials in general still remains an open question and a future research direction of both the nanomaterials and biomedical research communities.

4.2 Summary and Conclusions on 3-D PZT and Electrode Thin Film Stack

4.2.1 Electrode Fabrication

The most widely used sol-gel method for $LaNiO_3$ thin film fabrication utilizes lanthanum nitrate and nickel acetate, the latter of which is relatively costly [80, 81]. In this study, a sol-gel route employing lanthanum nitrate and cheaper nickel nitrate was used to synthesize $LaNiO_3$ electrodes directly on Si wafers. The critical thickness above which cracking will occur is inferred to be around 200 nm for films synthesized by this process. A resistivity of $1.2\times10^{-3}\Omega\cdot cm^{-1}$ has been achieved with a 500 ℃ anneal in air for 1 hour. Moreover, a slightly higher resistivity of $4.4\times10^{-3}\Omega\cdot cm^{-1}$ has been achieved with a 600 ℃ anneal in oxygen for only 1 min in an RTP furnace. The obtained conductivity from a 1 min anneal is comparable to the value obtained by Miyake et al. whereas in their study, nickel acetate was used, and a higher temperature (700 ℃) and longer annealing time (10-20 min) was employed to achieve satisfying conductivity.

4.2.2 PZT and PLZT Thin Film Fabrication

High quality PZT and PLZT thin films have been synthesized by sol-gel method and deposited on Pt and $LaNiO_3$ electrodes.

As a high dielectric constant material, PZT is intrinsically more prone to defects than simple oxides and nitrides with a much lower dielectric constant. Moreover, traditionally, the PZT thin films produced by the sol-gel method are considered to be of lower quality and prone to defects, pinholes and precipitations. As a result, most characterization was done on device areas on the order of 10^{-1}-$10^{-2}mm^2$. In this study, the yield of sol-gel

synthesized PZT thin films over a large area is characterized. A high capacitance density of 4μF/cm^2 was achieved on 400 nm films with high breakdown voltage and a high yield of 98% on 0.28 mm^2 devices. 14% yield has been achieved with 7.18 mm^2 devices. The dielectric constant of the fabricated PZT thin film is 2.3 times of the PZT films that are commercially used for Samsung 4Mbit FeRAM devices under the testing frequency of 100 kHz. The effect of temperature and applied bias on capacitance density has also been characterized.

With PLZT, a new approach using PZT capping layer to ensure phase purity of the film was employed. The PZT capping layer is ferroelectric itself, thus it gives better performance than the approach proposed by Tania *et al.* [25] in which a non-ferroelectric PbO capping layer was used. A PZT buffer layer is also found to alter the crystal orientation of the PLZT and be beneficial for its electrical performance. Also, addition of PLZT was found to double the breakdown voltage compared to pure PZT without sacrificing the capacitance density. The mechanism of such a reliability improvement can be attributed to the reduction of oxygen vacancy concentration after La addition. Employing the PZT/PLZT/PZT sandwiched structure, the breakdown voltage of the 400 nm thick film was increased to twice of that of the PZT films of the same thickness without sacrificing much of the capacitance density. A capacitance density of 3.5μF/cm^2 was achieved with breakdown voltage of 49V and yield of 92% on 0.28 mm^2 devices.

Compatibility of PZT with $LaNiO_3$ electrode has been demonstrated with a slight degradation of electrical properties. Possible optimization of the process has been suggested to improve the compatibility of the two materials.

4.2.3 3-D Conformal Coating with a Low-cost, High Throughput Solution Based Process

Low-cost, conformal thin film coating on 3-D surfaces was demonstrated with Si trenches with their orientation parallel to the spinner radial direction for the first time. Step coverage of 100% was demonstrated with reasonably conformal coating thickness. This demonstrates that the sol-gel technology on planar devices is extensible to 3-D surfaces and opens up potential device possibilities for both capacitor and MEMS applications.

4.3 Summary and Conclusions on ZnO and GaN Nanowire Devices

4.3.1 Fabrication and Measurement on ZnO Microwire Photocells

The electrical response of single ZnO microwire photocells with (1) two Schottky contacts and (2) two Ohmic contacts has been measured. The current output was highly dependent on the excitation position, with the current gradually switched polarity as the illuminated area scanned through the whole microwire. There was a null point on the nanowire where the two currents that flowed in the opposite directions canceled each other. The observed phenomena were attributed to the competition between the two opposite photocurrents and thermoelectric currents, generated at the two nanowire-electrode junctions.

The current was also found to be polarization dependent, and the dependence was slightly more obvious at higher excitation intensities. When the excitation polarization was perpendicular to the wire axis, the current was higher than that obtained with the excitation polarization parallel to the axis. The effect of wire dimension was excluded due to the relative larger thickness of the wire with respect to the excitation wavelength. The effect of excitation polarization was attributed to the difference in light absorption due to crystal anisotropy.

4.3.2 Fabrication and Characterization of Strain-sensitive GaN Nanowire Devices

GaN nanowires were synthesized on both r-sapphire and c-GaN substrates. The effect of substrate material and substrate position was qualitatively discussed. c-GaN substrates were found to be beneficial for nucleation and produced higher nanowire densities with a three-fold symmetric alignment, due to better lattice match. Electrical characterization of single GaN nanowire devices has also been carried out, and the strain response of these nanowire devices has been tested. The I-V characteristics of a single GaN nanowire connected by two electrodes with Schottky contacts can be effectively tuned by the applied strain, which is the first report on GaN piezotronic devices. The observed I-V characteristic change was attributed to the Schottky barrier height change due to strain-induced piezopotential in the GaN crystal.

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